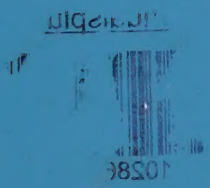


EIP Microwave

A JENOA COMPANY

MANUAL CHANGE INFORMATION
MODEL 331

At EIP we continually strive to keep up with the latest electronic developments by adding circuit and component improvements to our instruments as soon as they are developed and tested.

Sometimes, due to printing and shipment requirements, we can't get these changes immediately into printed manuals. As a result, your instrument may contain some or all of the changes listed below.

FEBRUARY 1979

PAGE NUMBER

6-4 EXT. TRIG. - A203TP8 should read A203TP5.

6-5 EXT. TRIG. - A203TP8 should read A203TP5.

6-6 Step 8 should read "……..reset at 50% (1 div.) of the ……."

7-3 A106 High Frequency should be listed as part number 2020068.

7-3 A113 Counter Interconnect Board should be listed as EIP part number 2020069.

102-3 U20 should have part number 3087432, and manufacturing number DM74LS32.

104-7 P1 pins 6, 7, & 8 (Bands, 1, 2, & 3 Select) should be overscored to denote a negative condition.

106-3 C6, C14, and C16 are now part number 2300029.

106-4 Q7 has been changed to part number 4710026.

106-5 R41 is now part number 4130200, 20 ohms, 2%.

106-5 U4 TYP MFG No should read DM74LS04. Delete the "N".

106-7 Change Q7 to part number 4710025.

Change R41 to read 20 ohms, 2%.

107-2 Change C1 value to 9500 uF, 25V, part number 2200016.

Change C5 value to 44,000 uF, 15V, part number 2200018.

107-2 C9 and C13 have been changed to "Tant, 33 uF, 20V" with part number changed to 2300023.

107-3 Change R20 to Met Ox, 5.6K, 2%, Part number 4130999 SAT.

107-5 Change Q7 and Q10 to read MJE3055.

Change Q6 to read MJE3070.

Change R20 to 5.6K, 2%.

107-5 Change C9 and C13 to read 33uF, 20V.

201-7 U5 should have a TYP MFG No that reads LM741CN.

202-2 Last paragraph, line 2 should read "U10 divides the line from 1 to 9.8 GHz……".

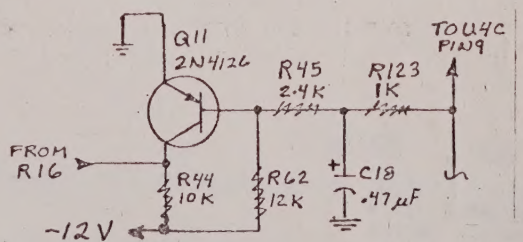
202-3 Add C18, Tant, .47uF, part number 2300005.

202-4 Change R45 to Met Ox, 2.4K, 2%, part number 4130242.

202-6 Add R123, Met Ox, 1K, 2%, part number 4130102.

202-9 U4B pin 5. delete overscore on "CLOCK ENABLE".

Change schematic as shown.



203-11 Delete overscore on "CLOCK ENABLE" between P1 pin 8 and U9A pin 6.

204-4 Change Q1 to NPN, RF (2N5179), part number 4710026, (Qty.1).

Mark schematic (pg 204-9) with change.

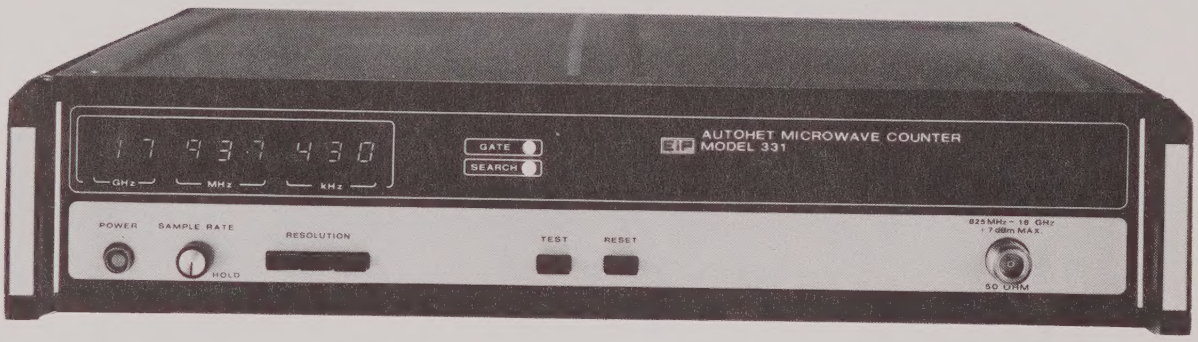
SEE 2

THE FOLLOWING TABLE PROVIDES PIN INFORMATION FOR EACH IC DEVICE USED IN THE 331 COUNTER.

IC	GND	+5V	-5.2V	+12V	-12V
DM74LS00	7	14			
DM74LS01	7	14			
DM74LS02	7	14			
DM74LS03	7	14			
DM74LS04	7	14			
DM74LS05	7	14			
DM74LS08	7	14			
DM74H08N	7	14			
DM74LS11	7	14			
DM74LS20	7	14			
DM74LS32	7	14			
DM74LS42	8	16			
DM74LS47	8	16			
DM74LS54	7	14			
DM74LS73	11	4			
DM74LS75	12	5			
DM74LS76	13	5			
DM74LS90	10	5			
DM74LS93	10	5			

IC	GND	+5V	-5.2V	+12V	-12V
DM74LS123	8	16			
DM74123	8	16			
DM74LS153	8	16			
DM74LS155	8	16			
DM74LS176N	7	14			
DM74196N	7	14			
DM74LS393	7	14			
DM8097N	8	16			
DM8601N	7	14			
MC10105L	1, 16				
MC10131L	1, 16		8		
MC1039P	16	1	8		
MK5009P	2	15			16
NE5534N				7	4
NE555V	1	8			
SP8637B	12		5		
SP8657B	2		5		

331 CCN 310 S/N 6
OPT 39/T32



Model 331
Autohet Microwave Counter

$946 5700

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List of Effective Pages

This List of Effective Pages gives the most recent date on which the technical material on any given page was altered. If a page is simply rearranged due to a technical change on a previous page, it is not listed as a changed page. Within the manual, changes are marked with a vertical bar in the margin.

Pages	Effective Date
First Edition	Aug 1978

Printing History

New editions incorporate all update material since the previous edition. The date on the title page changes only when a new edition is published. If minor corrections and updates are incorporated, the manual is reprinted but the date and edition number on the title page do not change.

First Edition . . . . . Aug 1978

Certification

EIP Microwave certifies that this instrument was thoroughly inspected and tested, and found to be in conformance with the specifications noted herein at time of shipment from factory.

Warranty

EIP Microwave warrants this counter to be free from defects in material and workmanship for one year from the date of delivery. Damage due to accident, abuse, or improper signal level, is not covered by the warranty. Removal, defacement, or alteration, of any serial or inspection label, marking, or seal, may void the warranty. EIP Microwave will repair or replace at its option, any components of this counter which prove to be defective during the warranty period, provided the entire counter is returned PREPAID to EIP or an authorized service facility. In-warranty counters will be returned freight prepaid; out-of-warranty units will be returned freight COLLECT. No other warranty other than the above warranty is expressed or implied.

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Table of Contents

Page

Section 1, General Information and Specifications 1-1
- 1-1. Description 1-1
- 1-2. Instrument Identification 1-1
- 1-3. Specifications 1-2

Section 2, Installation 2-1
- 2-1. Unpacking 2-1
- 2-2. Installation 2-1
- 2-3. Incoming Operational Check 2-1

Section 3, Operation 3-1
- 3-1. Front Panel Controls, Indicators and Connectors 3-1
- 3-2. Rear Panel Connectors 3-2
- 3-3. Display Brightness Adjustment 3-2

Section 4, Theory of Operation 4-1
- 4-1. General 4-1
- 4-2. 300 MHz Direct Counter 4-2
- 4-3. Autohet Converter 4-3
- 4-4. An Introduction to YIG Filters 4-4

Section 5, Maintenance, Service and Troubleshooting 5-1
- 5-1. Maintenance 5-1
  - Fuse Replacement 5-1
  - Air Circulation 5-1
- 5-2. Counter Servicing 5-1
  - Recommended Procedures 5-1
  - Servicing Precautions 5-2
- 5-3. Factory Servicing 5-2
  - Pack The Counter 5-4
- 5-4. Troubleshooting 5-4
  - Malfunction 5-4
  - Failure to Indicate All Zeros 5-5
  - Malfunction Self-Test 5-5
  - Converter Malfunction 5-6

Section 6, Adjustments and Calibration 6-1
- 6-1. General 6-1
- 6-2. Power Supply Adjustments 6-2
- 6-3. Video Detector Gain Adjustment 6-2
- 6-4. In-Band Detector Adjustment 6-3
- 6-5. Comb Leveling, Bias, and Threshold Adjustment 6-4
- 6-6. YIG Driver Offset and Slope Adjustment 6-5

Table of Contents, continued

Page

Section 6, Adjustments and Calibration (Continued)

6-7. YIG Delay Correction 6-7
6-8. Optional Video Detector Gain Adjustment 6-8
6-9. Final Comb Leveling/Bias 6-8
6-10. Time Base Calibration 6-10
6-11. Temperature Compensated Crystal Oscillator (TCXO) Calibration 6-11
6-12. Range and Sensitivity Performance Test 6-12

Section 7, Functional Description and Illustrated Parts Breakdown 7-1

7-1. Reference Designators 7-2
7-2. Abbreviations 7-2
7-3. 331 Counter (Top Assembly) Parts List 7-3
7-4. Assembly Locations and Cable Interconnections 7-5
7-5. Introduction to Count Chains 1, 2 and 3 7-7

A101 Count Chain 1 101-1
A102 Count Chain 2 102-1
A103 Count Chain 3 103-1
A104 Control 2 104-1
A105 Control 1 105-1
A106 High Frequency 106-1
A107 Power Supply 107-1
A108 Reference Oscillator Buffer 108-1
A110 Display 110-1
A113 Counter Interconnection (Mother Board) 113-1
A201 Source Amplifier 201-1
A202 Converter Control 2 202-1
A203 Converter Control 1 203-1
A204 Video Amplifier 204-1
A208 Converter Interconnect 208-1

Section 1
General Information and Specifications

1-1. DESCRIPTION

The EIP 331 Autohet Microwave Counter automatically measures the frequency of any CW signal within the range of 825 MHz to 18.0 GHz. Measurements are made by heterodyning the input frequency with an automatically selected harmonic of an internal 200 MHz comb generator, producing a difference frequency which falls within the range of a 300 MHz direct counter. The inaccuracy of the reading indicated by the counter is directly related to the quality of the Time Base Oscillator over the entire operating range of the counter. (Refer to Section 6.)

The display on the counter gives a direct readout of the measured frequency over the entire operating range of the counter. The counter also includes automatic suppression of leading zeros, except during a no signal condition.

The frequency readout of the counter is displayed in a fixed position format that is sectionalized in GHz, MHz and KHz.

To assure trouble-free performance, the 331 Counter is completely solid-state. The major portion of the circuitry is contained on plug-in printed circuit boards or in easily removed modules for ease of operation and maintenance. Special test points allow monitoring of critical circuit functions.

NOTICE

"AUTOHET is a registered trademark of EIP.

1-2. INSTRUMENT IDENTIFICATION

The Model 331 Autohet Microwave Counter is identified by two number sets; the model and configuration number (e.g., 331-CCN101) and a serial number (e.g., 12345). Both sets of numbers should be mentioned in any correspondence regarding the counter.

1-3. SPECIFICATIONS

GENERAL

Frequency Range	825 MHz to 18.0 GHz
Accuracy	±1 count ±time base error
Resolution	1 KHz to 1 MHz in decade steps
Gate Time	1 ms
Sample Rate	Variable 10 Hz to 0.1 Hz with switchable HOLD
Display	8 Digit LED, sectioned in GHz, MHz and KHz
Acquisition Time	10 ms/GHz +50 ms nominal (Once locked, readings can be at select sample rate. With sample rate disabled, maximum rate is 800 readings/second.)
Operating Temp.	0° to +50° C
Power	115/230 Vac, ± 10%, 50-60 Hz, 80 watts nominal
Shipping Weight	30.0 lbs (13.6 kg)
Net Weight	25.5 lbs (11.6 kg)
Accessories Furn.	Detachable power cord, 8 ft (241 cm) long, with plug Operating and Service Manual
Accessories Avail.	Rack Mount Kit P/N 2010008 Carrying Case P/N 5700001 Calibration Kit P/N 2000005

TIME BASE

Type	TCXO
Crystal Frequency	10 MHz
Aging Rate	$< \lvert 3\times10^{-7} \rvert$/month
Short Term Stability	$< \lvert 1\times10^{-9} \rvert$rms for 1 sec avg time
Temperature	$< \lvert 2\times10^{-6} \rvert$ between 0° to +50° C
Line Variation	± 10% line volt. change results in frequency shift of $< \lvert 1\times10^{-7} \rvert$
Warm Up Time	None
Output freq.	10 MHz square wave, 1 VP.P min into 50 ohms

SIGNAL INPUT

Frequency Range	825 MHz to 18.0 GHz
Min. Sensitivity	825 MHz to 1.1 GHz, -15 dBm (40 mV rms) 1.1 GHz to 12.4 GHz, -20 dBm (22 mV rms) 12.4 GHz to 18.0 GHz, -15 dBm (40 mV rms)
Maximum Input	+7 dBm (0.5 V rms) for proper operation +20 dBm (2.2 V rms) without damage
Input Impedance	50 ohms nominal
Coupling	DC
Connector	Type N Precision, female
VSWR	2.5: 1 typical
FM Tolerance	40 MHz p-p worst case for modulation rates from dc to 10 MHz

Section 2
Installation

2-1. UNPACKING

Carefully inspect the shipping carton for any evidence of damage before opening. If any seems apparent, ask that the shipper's agent be present when the instrument is unpacked.

Remove the packing carton and supports, being careful not to scar or damage the instrument. Make a complete visual inspection of the counter. Check for any damage or missing components. Check that all switches and controls operate mechanically. Report any damage to EIP immediately.

2-2. INSTALLATION

There are no special installation instructions for the 331 Counter. The unit is self-contained bench or rack mounted instrument, which only requires connection to a standard, single-phase, 115/230 V, 50-60 Hz power line for operation.

CAUTION

Check current rating of counter fuse and setting of rear panel 115/230 Vac slides switch before applying power to counter.

2-3. INCOMING OPERATIONAL CHECK

The following procedure outlines an operational check of the counter which may be conducted without special tools, signal generators, or test equipment. The internal TIME BASE CLOCK is used as the input signal to the 300 MHz counter, therefore, it cannot check the operation of the converter section.

1. Turn counter POWER switch off. Check fuse rating and setting of 115/230 switch (on rear panel).

2. Connect counter power cord to a source of 115 or 230 V, 50-60 Hz, single-phase power. The ground terminal on the power cord plug should connect to a reliable earth ground.

3. Press POWER switch (on front panel) to turn counter on. The counter display should light, and the internal cooling fan should operate.

4. Partially depress any one of the RESOLUTION switches and release it so no switch remains in the depressed position. All digits in the 8-digit display should indicate "0" (zero).

5. Depress the TEST switch on the front panel. The display should indicate 10 000 (10 MHz). Note that the three leading zeros are blank (not lit).

6. Blank the 1 KHz digit by pressing the right hand RESOLUTION switch.

7. Depress the TEST button again. The display should still indicate 10 MHz, but with final "0" blanked.

8. Test each RESOLUTION switch in turn, starting with the 1 KHz digit. Note that the digit immediately above that switch, and all digits to the right of that switch are blanked.

9. Unblank all display digits (see step **4** for procedure).

10. With no input signal, the entire display should show all zeros.

11. Depress both the TEST and RESET switches simultaneously. All display digits should show "8" (all segments of each display lighted).

This completes the counter check. All CW signals within the frequency range of the counter may be counted as required. Refer to Section 1 for proper signal levels. If counter fails to perform as described above, refer to Section 5.

Section 3
Operation

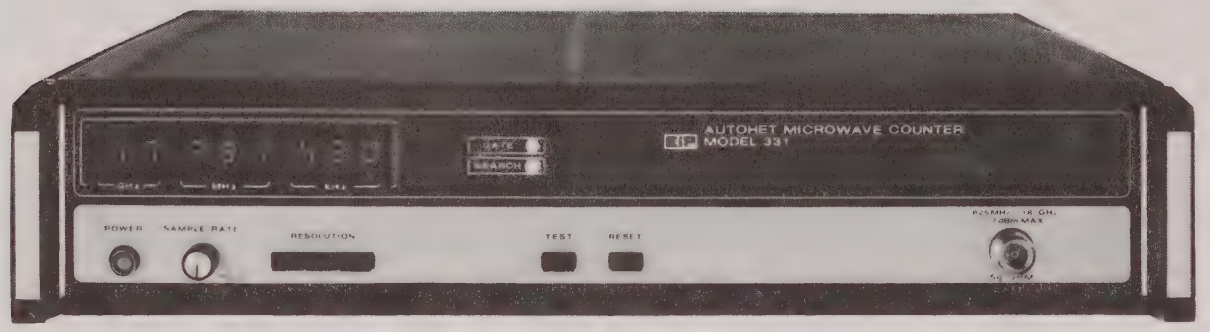


Figure 3-1. Front Panel

3-1. FRONT PANEL CONTROLS, INDICATORS and CONNECTORS

- POWER switch turns counter on and off.
- SAMPLE RATE/HOLD varies time between measurements from 1/10 to 10 seconds per reading. Gate time is added to sample time. Last reading is retained indefinitely in HOLD.
- RESOLUTION pushbuttons switches (3) allow blanking (turning off) the three least significant digits in the display. Each switch blanks the digit directly above it, and all digits to the right. 1 KHz resolution is achieved by partially depressing and releasing one of the switches, thereby releasing all of the switches.
- TEST places the counter in self-test mode with signal from the internal 10 MHz Time Base. Proper display is 10,000 (10 MHz).
- RESET manually over-rides all controls, resets the counter and converter, and initiates a new reading.
- The 8-digit LED (light-emitting diode) display provides a numerical readout of the input frequency. To test the display, press TEST and RESET simultaneously. All digits will light and display number "8".
- GATE indicator lights when the signal gate is open.
- SEARCH indicator remains lit when the converter is not locked to an input signal.
- The signal input connector (precision type N, female) is used for measurements between 825 MHz and 18 GHz.

WARNING

DO NOT APPLY ANY SIGNAL THAT EXCEEDS THE MAXIMUM INPUT SPECIFIED. EXTENSIVE DAMAGE WILL OCCUR WHETHER THE COUNTER IS TURNED ON, TURNED OFF, OR APPEARS TO BE INOPERATIVE. THIS DAMAGE IS NOT COVERED BY THE WARRANTY.

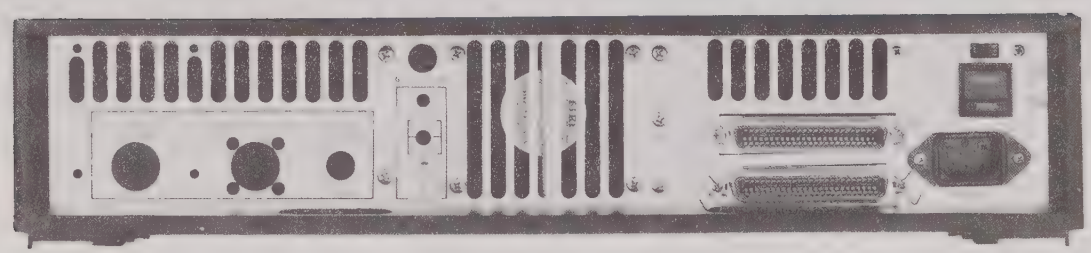


Figure 3-2. Rear Panel

3-2. REAR PANEL CONNECTORS

- TIME BASE/10 MHz connector (type BNC, female) allows monitoring of internal 10 MHz Time Base.
- BCD OUTPUT (J2) connector is used with Option 39. Refer to Appendix B (Options) for complete description.
- Programming (J3) connector is used with Option 31.
- AC POWER connector accepts power cord supplied with counter.
- FUSE provides overload protection. Use only 1.5 A, Slow-blow, 3AB/MDX type fuse for 115 Vac operation. For 230 Vac operation use a 0.75 A slow-blow, 3AB/MDL type fuse.
- 115/230 switch sets operating voltage of counter to match power line.

CAUTION

Be sure 115/230 switch setting and fuse rating match power line voltage.

3-3. DISPLAY BRIGHTNESS ADJUSTMENT

The numerical display brightness may be adjusted. The potentiometer R20, located on PC board A103, is accessable by removing the top cover of the counter. A clockwise adjustment will increase brightness, and counter-clockwise will decrease brightness.

Section 4
Theory of Operation

4-1. GENERAL

The 331 Counter automatically measures and displays the frequency of any CW signal from 825 MHz to 18 GHz.

An Autohet Converter translates the input frequency downward into the range of a 300 MHz direct counter. This is accomplished by mixing the input signal with a single known harmonic of the counter Time Base oscillator, to produce a difference frequency which can be counted. The frequency of the known harmonic is added to the counted signal to obtain the input frequency.

Figure 4-1 shows a block diagram of the complete 331 Counter. Figure 4-2 shows a block diagram of the Autohet Converter. Detailed theory and circuit descriptions of the direct Counter and the Converter subassemblies are given in Section 7.

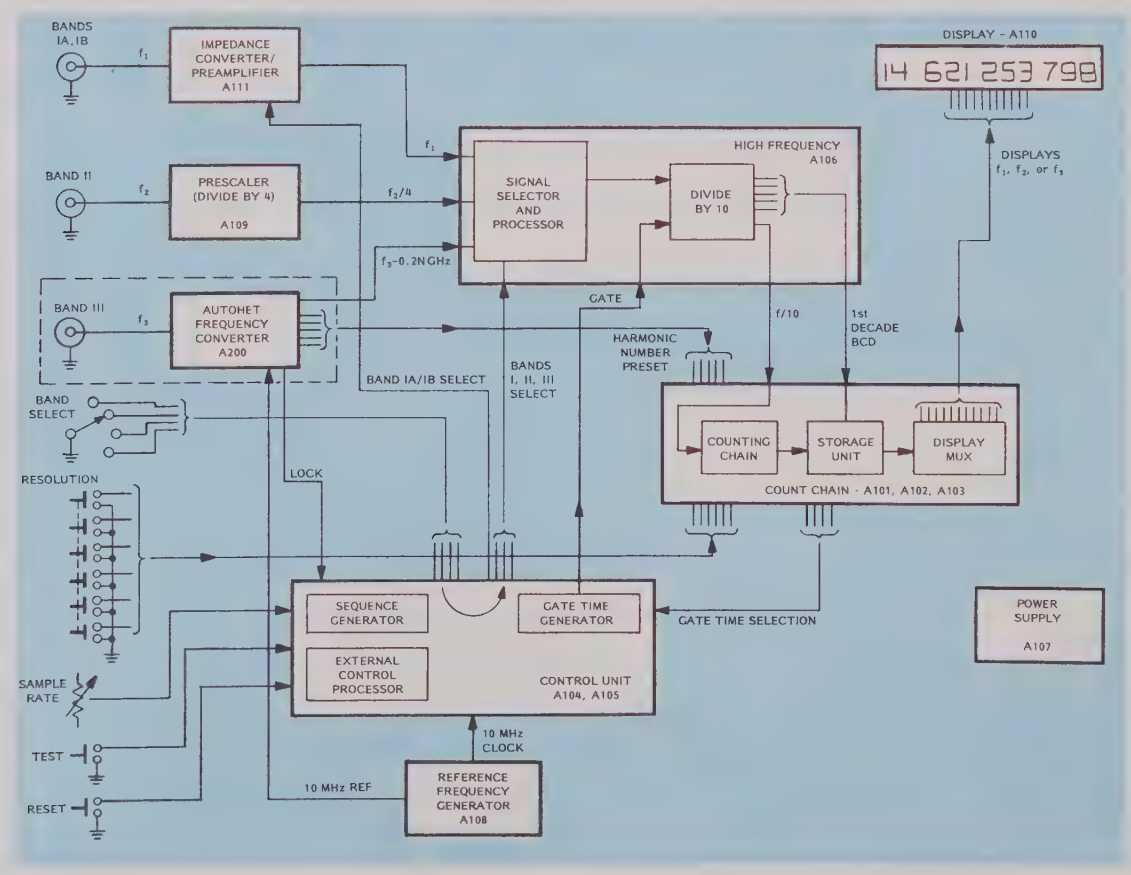


Figure 4-1. Counter Block Diagram

The counter operation is best described by separating the instrument into two distinct functions, the Direct Counter and the Autohet Converter. These functions are interconnected in two significant areas:

- presetting the counter to the appropriate harmonic number.
- counting the heterodyned difference frequency from the Converter by the Direct Counter.

4-2. 300 MHz DIRECT COUNTER

The frequency measurement by the Direct Counter is made by accumulating the number of input events (cycles of a sine wave), which occur within a precisely determined time interval. This time interval is based on the frequency of the Time Base Oscillator.

The 300 MHz Direct Counter is physically separated into several subassemblies, designated A101 through A111 (see Figure 4-1). The subassemblies are tied together via the Counter Interconnect Board (A113). The counter is divided functionally in approximately the same manner as it is divided into subassemblies. Count Chain Boards A101, A102 and A103 operate functionally as a single unit, as do the Control Boards A104 and A105. The principal interconnections are shown in Figure 4-1.

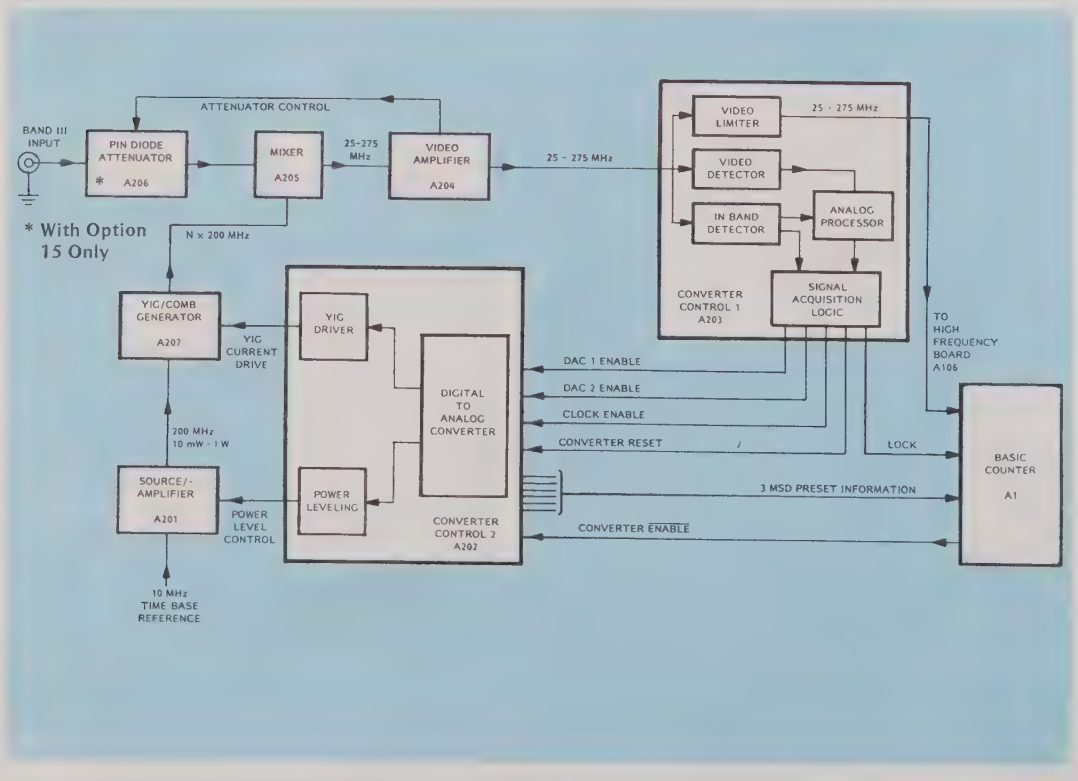


Figure 4-2. Autohet Converter Block Diagram

The signal input to the 331 Counter is translated by the Autohet Converter into the range of 25 to 275 MHz, and routed to the High Frequency Board.

The High Frequency Board (A106) receives the input signal from one of the processors, squares the signal, and forms it into a train of constant duration pulses. This pulse train frequency is then divided by ten, and sent to the Count Chain.

The Control 1 and Control 2 Boards (A104 and A105) contain circuitry to guide the counter through the steps necessary to acquire and display the input frequency. The circuits control the opening and closing of the signal gate in the High Frequency Board, and accept programming commands from the Converter, front panel controls, and the remote programming options.

The Count Chain Boards (A101, A102 and A103) accumulate the frequency from the High Frequency Board, store the accumulated information, and multiplex the stored information into a form usable by the Display Board (A110), which provides a visual display of the input frequency to the counter.

The Reference Oscillator Buffer (A108) produces a time base reference signal from the 10 MHz TCXO oscillator. All input frequencies to the counter are measured with respect to this signal.

The Power Supply (A107) provides regulated +12, -12, +5, -5.2 Vdc; and unregulated +18 Vdc.

4-3. AUTOHET CONVERTER

The Autohet Converter assembly translates the microwave frequencies at the signal input into the range of the Direct Counter. This translation is made by mixing the input signal with a known reference frequency, then amplifying the difference. The incoming frequency is determined by counting the difference frequency and adding it to the reference frequency.

The reference frequency is an integral multiple of 200 MHz derived from the 10 MHz Time Base Oscillator, and maintains counter accuracy in the microwave band.

The input signal passes through the 3dB Input Attenuator (A206) and is combined in the Mixer (A205) with the reference frequency from the YIG Comb Generator.

The YIG Comb Generator (A207) contains a Comb Generator and a YIG filter. The Comb Generator contains a step recovery diode to convert the 200 MHz sine wave input from the Source Amplifier (A201) into a train of narrow pulses containing all the harmonics of 200 MHz up to 18 GHz. This pulse train is then passed through a pair of YIG resonators which select the desired harmonic. The resonant frequency of the two-stage filter is proportional to a magnetic field generated by passing a current through a pair of coils.

The Source Amplifier (A201) contains an LC oscillator operating at 200 MHz (which is phase-locked to the 10 MHz Time Base Oscillator, A116). This 200 MHz signal is amplified to produce up to one watt of power to drive the Comb Generator (part of A207).

The Mixer (A205) is an integrated microwave strip-line assembly, containing a 3 dB hybrid coupler, a termination, a mixer diode, a matching network, a broadband DC return, and a bypass capacitor to separate the RF and IF signals. The Mixer produces two output signals; an IF signal (with frequency equal to the difference of the reference and incoming signals), and a DC signal (resulting from rectification of the total power applied to the mixer diode).

The IF signals from A205 enters Video Amplifier (A204) where it is amplified.

The circuitry required to control the Autohet Converter is located on two Converter Control Boards (A202 and A203). They set the YIG filter (in the YIG Comb Generator, A207) to the correct harmonics of 200 MHz, and provide IF frequency and harmonic information to the direct counter.

The YIG filter passband is continuously tuned over the operating range until an appropriate signal is received from the Video Amplifier. The sweep is stopped when the YIG filter passband is centered on the desired harmonic. Converter Control 1 (A203) performs all the signal processing and provides digital commands to Converter Control 2 (A202), which contains the Digital to Analog converters and the current driver necessary to tune the YIG filter. A detailed functional description is described in Section 7.

4-4. AN INTRODUCTION TO YIG FILTERS

Highly polished spheres of single crystal YIG (yttrium-iron-garnet), have a property called ferrimagnetic resonance. Basically, the ferrimagnetic resonance phenomenon can be explained in terms of spinning electrons creating a net magnetic moment in each molecule of a YIG crystal (See Figure 4-3A). Viewing the material macroscopically, there is no net effect because the magnetic dipoles associated with each molecule are randomly oriented (See Figure 4-3B). The application of an external magnetic biasing field, H_{DC}, causes the magnetic dipoles to be aligned in the direction of the biasing field (see Figure 4-3C).

An RF field can be used to create an orthogonal magnetic force. If the frequency of the RF field coincides with the natural precession frequency, there is strong interaction called ferrimagnetic resonance (Figure 4-3D).

Figure 4-3E shows the basic elements of a YIG bandpass filter. The filter consists of a YIG sphere at the center of two loops. The two loops are perpendicular to each other and to the dc biasing field, HDC. One loop carries the RF input and the other the RF output. When the RF signal frequency is the same as the natural precession frequency of the YIG, there is

strong coupling between the input and output loops. Thus, RF can only pass through the YIG filter at resonance. The resonant frequency is a linear function of the magnetic biasing field, H_{DC}. Generally, H_{DC} is provided by locating the YIG spheres between the poles of an electromagnet, and tuned by varying the current to the magnetic coils.

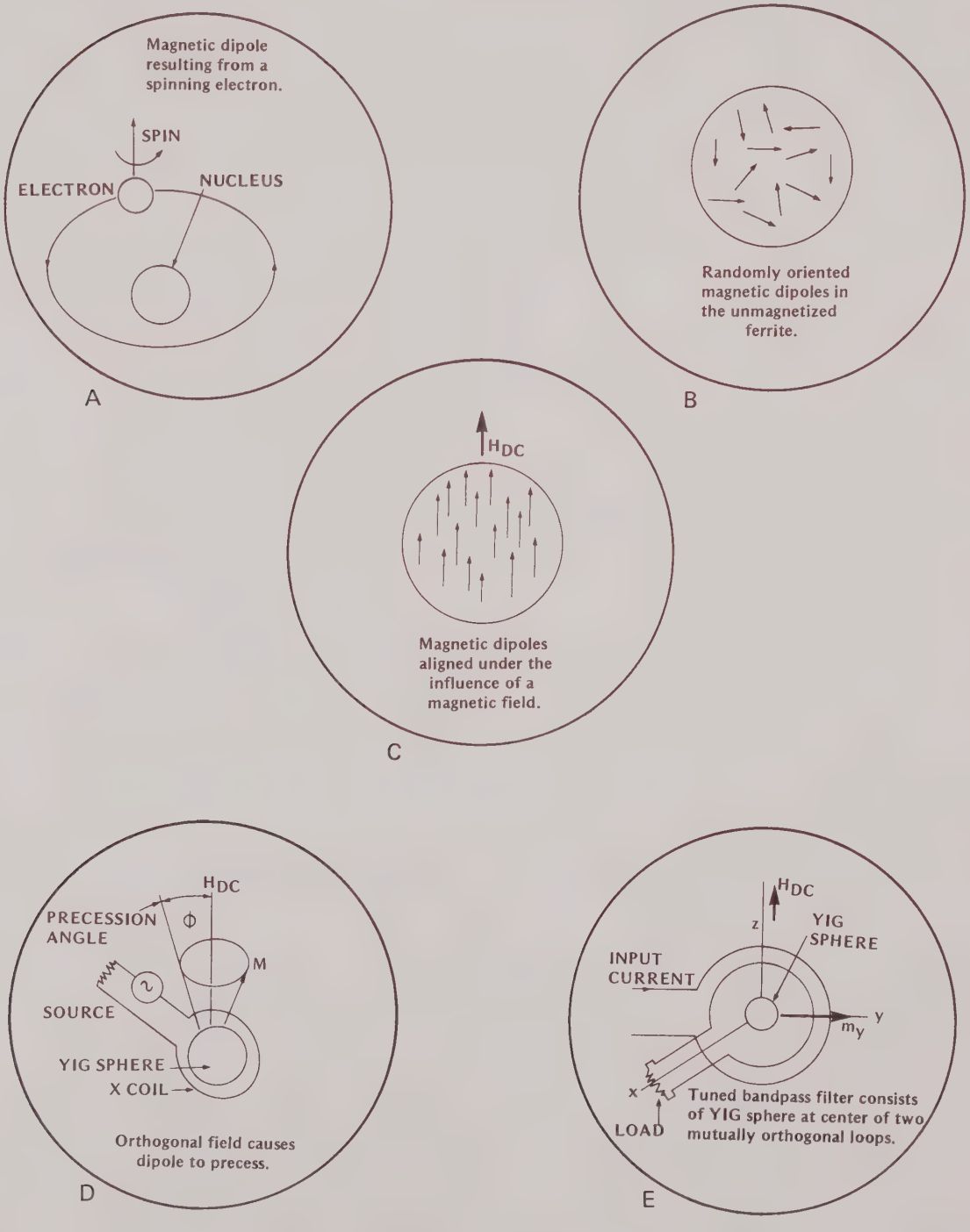


Figure 4-3. YIG Filters

Section 5
Maintenance, Service and Troubleshooting

5-1. MAINTENANCE

FUSE REPLACEMENT

The counter uses one fuse, located on the rear panel. For proper operation use only the fuse specified. Do not increase fuse rating or change fuse type. Set 115/230 slide switch (on rear panel) to match nominal power line voltage.

- For 115 Vac use a 1.5A, Slow-blow, 3AB/MDX fuse.
- For 230 Vac use a 0.75A, Slow-blow, 3AB/MDL fuse.

AIR CIRCULATION

During operation the internal fan draws in cooling air through the vents in the enclosure. Do not block enclosure vents or the temperature inside may rise, reducing counter stability and shortening component life.

5-2. COUNTER SERVICING

RECOMMENDED PROCEDURES

1. To remove plug-in PC boards, ease board out of socket by lifting up on board handles. Avoid placing strain on any connecting cables.

2. To unplug flat ribbon cables, turn off power to the counter. Use an IC extractor tool (P/N 5000094 or equivalent) to unplug connector.

3. To remove PCB socket locating key, key must be turned 90 degrees (before removal from, or insertion into socket) to avoid contact damage. Use long-nose pliers for removal and insertion.

4. A troubleshooting kit (P/N 2000005) is available for adjusting and repairing the counter. Contents include PCB extender cards, IC removal tool, Summing Amplifier, adapter cables and connectors.

5. Internal cable and harness routing is shown on a label attached to the top cover of the counter and in Section 7.

6. Circuit descriptions of PC boards and modular assemblies, the related schematic diagrams and component locator illustrations are shown in Section 7.

7. Troubleshooting diagrams (shown later in this section) are intended only as a guide, and do not describe every possible failure situation.

8. A list of test equipment recommended for servicing, calibration and performance testing, is given in Table 5-1. Other equipment may be used, but must perform equal to, or in excess of that listed.

9. A schematic diagram of a Summing Amplifier used in certain counter tests, is shown in Figure 5-1. This unit may be constructed by the user, or may be purchased from EIP (P/N 2010050).

SERVICING PRECAUTIONS

1. The Video Amplifier (A204) and the Source Amplifier (A201) should be replaced rather than being serviced in the field. Special test equipment and procedures are required for calibration.

2. If Converter Control 2 (A202) is repaired at EIP or in the field, recalibration must be made in its associated counter for proper counter operation.

CAUTION

Do not attempt repair or disassembly of the following components:

- YIG/COMB Generator (A207)
- MIXER (A205)
- INPUT ATTENUATOR (A206)
- TIME BASE OSCILLATOR (TCXO or OVEN Option)

5-3. FACTORY SERVICING

If the counter is to be returned to EIP for service or repair, *BE SURE TO INCLUDE THE FOLLOWING INFORMATION WITH THE SHIPMENT.*

1. Name and address of owner.

2. Model and complete serial number of counter.

Table 5-1. Recommended Test Equipment

EQUIPMENT DESCRIPTION	MFR.	MODEL	SECTION 5 SERVICE	SECTION 6 CALIBRATION & PERFORMANCE
Signal Source:				
(1) 825 MHz – 1 GHz	Wavetek	2001B	X	X
(2) 1 GHz – 18 GHz	S-D	521-series	X	X
Oscilloscope (Main Frame)	HP	180C	X	X
Dual Channel Ampl. (Plug-In)	HP	1801A	X	X
Delayed Time Base (Plug-In)	HP	1821A	X	X
Digital Voltmeter (4½ digit)	Dana	4800	X	X
Power Meter	HP	432B	X	X
Thermistor Mount (10 MHz-18 GHz)	HP	8478	X	X
Frequency Standard	HP	105A		X
VLF Comparator	HP	117A		X
Summing Amplifier	EIP	2010550	X	X
Variable 115 Vac Source	Staco	3PN501		X
Extender Card	EIP	2020021	X	X
Adapter Cable (SMC to BNC)	EIP	2040015	X	X
Misc. Attenuators, Adapters and Cables			X	X

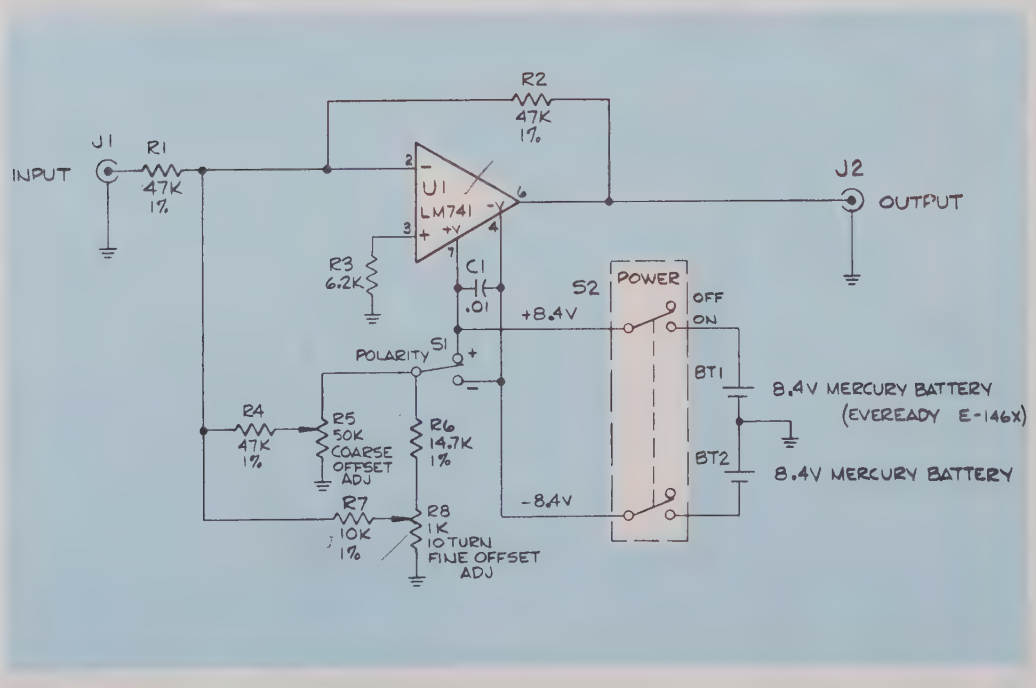


Figure 5-1. Summing Amplifier

3. *COMPLETE* description of trouble (e.g., Under what conditions did trouble occur? What was the signal level? What associated equipment was attached or connected to the counter? Did the equipment fail also?)

4. Name and telephone number of someone familiar with the problem who may be contacted by EIP.

5. Shipping address to which counter will be returned. Include any special shipping instructions.

NOTE

A counter repair and return form is bound into the back of this manual. If the form is missing, please supply all information requested.

PACKING THE COUNTER

1. Wrap the counter in plastic or heavy kraft paper, and repack in the original shipping container (if still available), using the original packing material.

2. If the original container and packing material is no longer available, use a heavy (275 lb. test) double-walled carton, with approximately 4" of suitable packing material between the inner and outer walls, with additional packing material as required between the counter and the inner carton. Seal with strong filament tape or strapping.

3. Make the shipping container to indicate that it contains fragile electronic instruments. Ship to EIP at address shown on title page of this manual.

5-4. TROUBLESHOOTING

MALFUNCTION AT TURN ON

If the counter fails to turn on (no display, no fan, etc.), check the following:

1. 115/230 switch at proper setting.

2. Power cord plugged into counter and into AC power source.

3. Correct AC power available at source.

4. Counter fuse good.

5. POWER switch in "ON" position. (Button depressed and green indicator showing.)

6. PC boards and connectors are properly engaged.

7. Counter power supply voltages correct (measured on Counter Interconnect, A113).

FAILURE TO INDICATE ALL ZEROS

If counter turns on, but fails to indicate all zeros with no applied signal, check that:

1. No RESOLUTION switches are depressed.

2. PC boards and connectors are properly engaged.

3. Counter Power Supply (A107) voltages are correct.

4. Perform Visual Display Test (Figure 5-2) by pressing TEST and RESET switches simultaneously. Display should show "8" in all decade positions.

5. If counter fails the Visual Display Test, refer to Figure 5-2. If counter displays all eights but a digit is missing, refer to Figure 5-3. If the display does not show all zeros when it should, refer to Figure 5-4.

MALFUNCTION IN SELF-TEST

If a counter turns on, but fails to indicate a reading of 10000 (10 MHz) in the test mode, check that:

1. Counter indicates all zeros with no applied signal.

2. PC boards and connectors are properly engaged.

3. Counter Power Supply (A107) voltages are correct.

4. Counter passes Visual Display Test.

5. Refer to Figure 5-5.

CONVERTER MALFUNCTION

If counter fails to read frequency correctly, check that:

1. A signal is applied to the signal input connector. The signal level and frequency should be the same as those specified in Section 1.

2. If signal input is correct, counter should indicate all zeros when signal is removed. If not, refer to Figure 5-2.

3. Counter passes Visual Display Test.

4. Counter operates correctly in test mode. See Figure 5-5.

5. Counter operates properly in Bands I and II.

6. Converter Control (A202 and A203) board connectors and coax cables are properly engaged. See Figure 5-6.

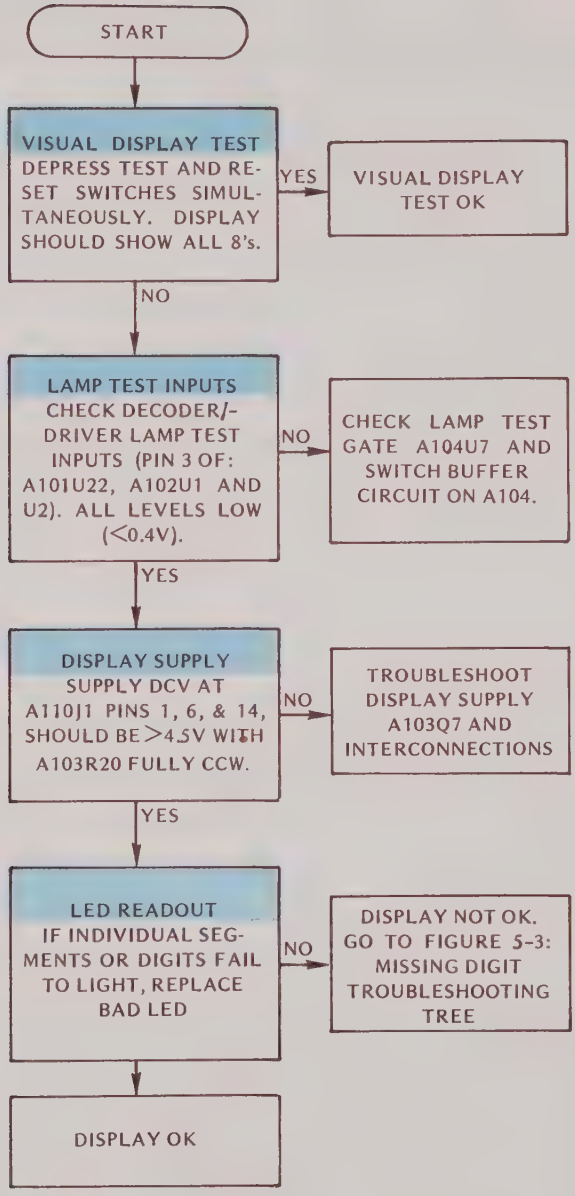


Figure 5-2. Visual Display Test

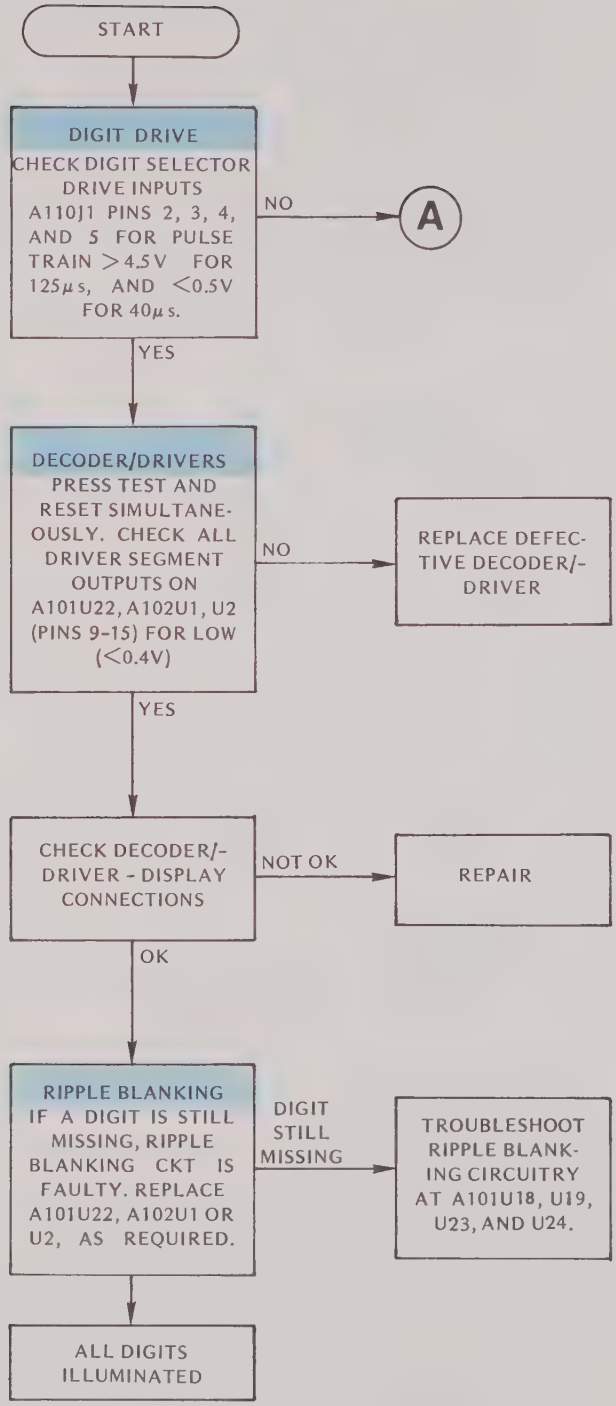

START
DIGIT DRIVE
CHECK DIGIT SELECTOR DRIVE INPUTS A110J1 PINS 2, 3, 4, AND 5 FOR PULSE TRAIN >4.5V FOR 125μs, AND <0.5V FOR 40μs.
NO
A
YES
DECODER/DRIVERS
PRESS TEST AND RESET SIMULTANEOUSLY. CHECK ALL DRIVER SEGMENT OUTPUTS ON A101U22, A102U1, U2 (PINS 9-15) FOR LOW (<0.4V)
NO
REPLACE DEFECTIVE DECODER/-DRIVER
YES
CHECK DECODER/-DRIVER - DISPLAY CONNECTIONS
NOT OK
REPAIR
OK
RIPPLE BLANKING
IF A DIGIT IS STILL MISSING, RIPPLE BLANKING CKT IS FAULTY. REPLACE A101U22, A102U1 OR U2, AS REQUIRED.
DIGIT STILL MISSING
TROUBLESHOOT RIPPLE BLANKING CIRCUITRY AT A101U18, U19, U23, AND U24.
ALL DIGITS ILLUMINATED

Figure 5-3. Missing Digit Test

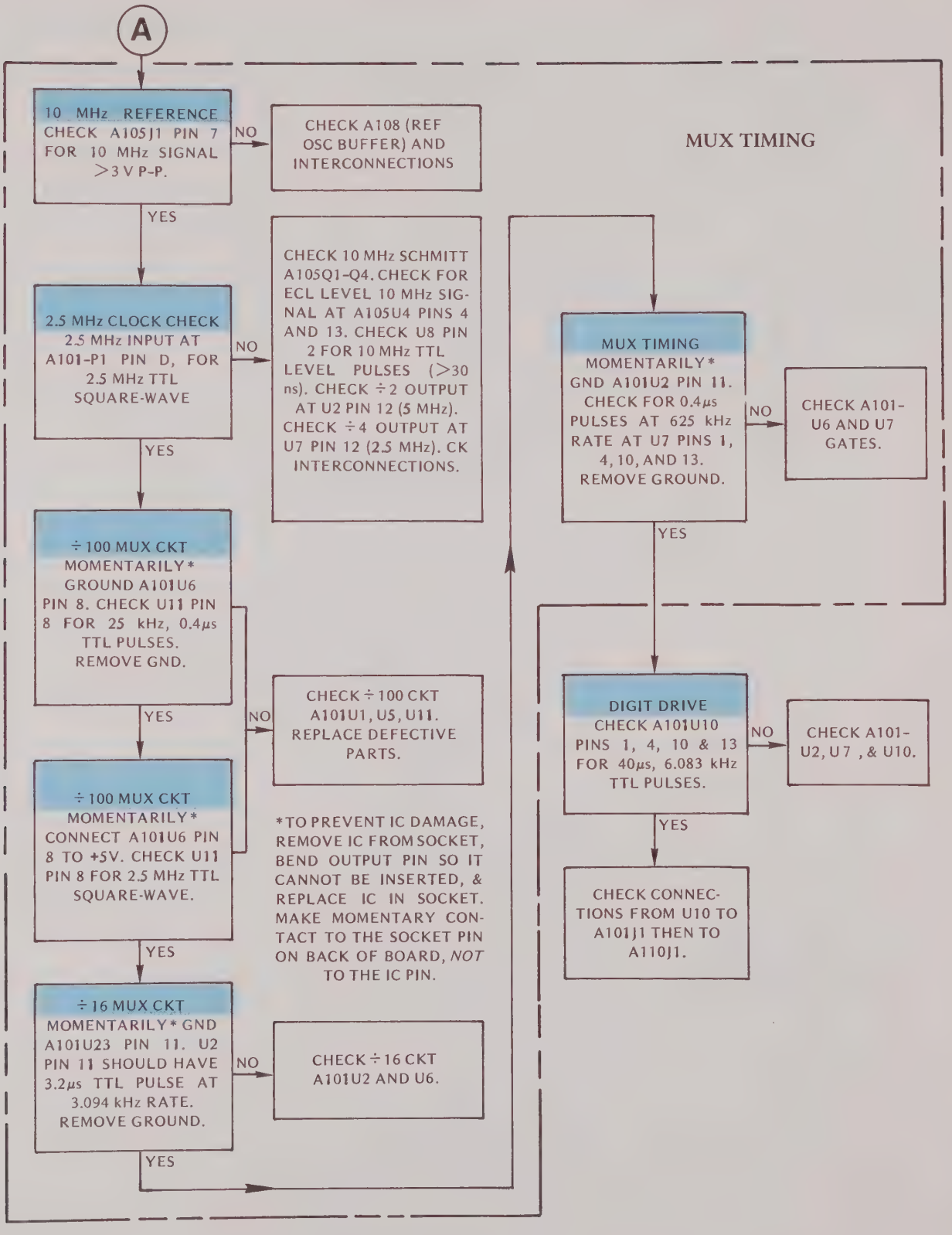

A
10 MHz REFERENCE CHECK A105J1 PIN 7 FOR 10 MHz SIGNAL >3 V P-P.
NO
CHECK A108 (REF OSC BUFFER) AND INTERCONNECTIONS
YES
2.5 MHz CLOCK CHECK 2.5 MHz INPUT AT A101-P1 PIN D, FOR 2.5 MHz TTL SQUARE-WAVE
NO
CHECK 10 MHz SCHMITT A105Q1-Q4. CHECK FOR ECL LEVEL 10 MHz SIGNAL AT A105U4 PINS 4 AND 13. CHECK U8 PIN 2 FOR 10 MHz TTL LEVEL PULSES (>30 ns). CHECK ÷2 OUTPUT AT U2 PIN 12 (5 MHz). CHECK ÷4 OUTPUT AT U7 PIN 12 (2.5 MHz). CK INTERCONNECTIONS.
YES
÷100 MUX CKT MOMENTARILY* GROUND A101U6 PIN 8. CHECK U11 PIN 8 FOR 25 kHz, 0.4µs TTL PULSES. REMOVE GND.
YES
NO
CHECK ÷100 CKT A101U1, U5, U11. REPLACE DEFECTIVE PARTS.
÷100 MUX CKT MOMENTARILY* CONNECT A101U6 PIN 8 TO +5V. CHECK U11 PIN 8 FOR 2.5 MHz TTL SQUARE-WAVE.
YES
*TO PREVENT IC DAMAGE, REMOVE IC FROM SOCKET, BEND OUTPUT PIN SO IT CANNOT BE INSERTED, & REPLACE IC IN SOCKET. MAKE MOMENTARY CONTACT TO THE SOCKET PIN ON BACK OF BOARD, NOT TO THE IC PIN.
÷16 MUX CKT MOMENTARILY* GND A101U23 PIN 11. U2 PIN 11 SHOULD HAVE 3.2µs TTL PULSE AT 3.094 kHz RATE. REMOVE GROUND.
NO
CHECK ÷16 CKT A101U2 AND U6.
YES
MUX TIMING
MUX TIMING MOMENTARILY* GND A101U2 PIN 11. CHECK FOR 0.4µs PULSES AT 625 kHz RATE AT U7 PINS 1, 4, 10, AND 13. REMOVE GROUND.
NO
CHECK A101-U6 AND U7 GATES.
YES
DIGIT DRIVE CHECK A101U10 PINS 1, 4, 10 & 13 FOR 40µs, 6.083 kHz TTL PULSES.
NO
CHECK A101-U2, U7 , & U10.
YES
CHECK CONNECTIONS FROM U10 TO A101J1 THEN TO A110J1.

Figure 5-3. Missing Digit Test (Continued)

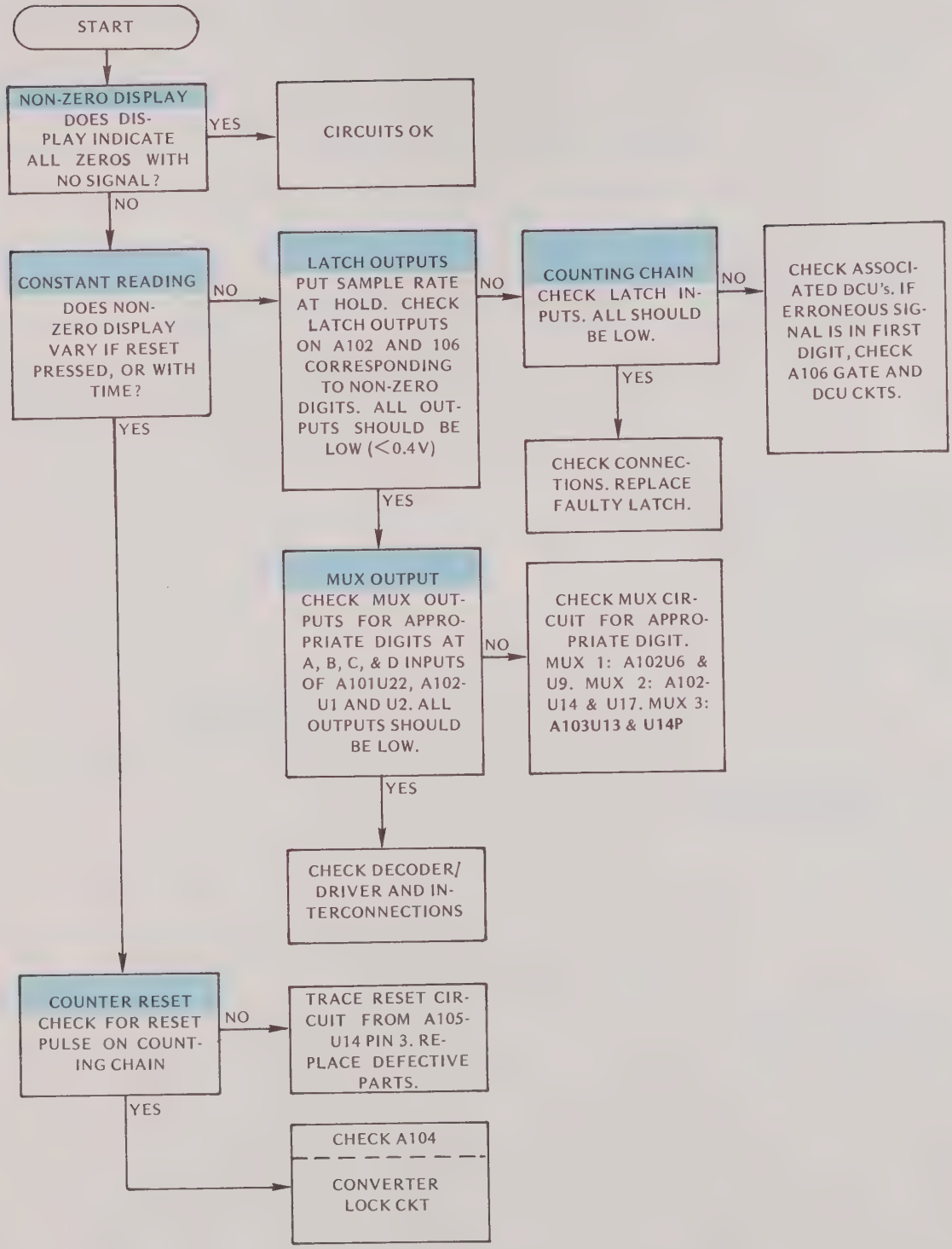

START
NON-ZERO DISPLAY
DOES DISPLAY INDICATE ALL ZEROS WITH NO SIGNAL?
YES
CIRCUITS OK
NO
CONSTANT READING
DOES NON-ZERO DISPLAY VARY IF RESET PRESSED, OR WITH TIME?
NO
YES
LATCH OUTPUTS
PUT SAMPLE RATE AT HOLD. CHECK LATCH OUTPUTS ON A102 AND 106 CORRESPONDING TO NON-ZERO DIGITS. ALL OUTPUTS SHOULD BE LOW (<0.4V)
NO
YES
COUNTING CHAIN
CHECK LATCH INPUTS. ALL SHOULD BE LOW.
NO
YES
CHECK ASSOCIATED DCU's. IF ERRONEOUS SIGNAL IS IN FIRST DIGIT, CHECK A106 GATE AND DCU CKTS.
CHECK CONNECTIONS. REPLACE FAULTY LATCH.
MUX OUTPUT
CHECK MUX OUTPUTS FOR APPROPRIATE DIGITS AT A, B, C, & D INPUTS OF A101U22, A102-U1 AND U2. ALL OUTPUTS SHOULD BE LOW.
NO
CHECK MUX CIRCUIT FOR APPROPRIATE DIGIT. MUX 1: A102U6 & U9. MUX 2: A102-U14 & U17. MUX 3: A103U13 & U14P
YES
CHECK DECODER/ DRIVER AND INTERCONNECTIONS
COUNTER RESET
CHECK FOR RESET PULSE ON COUNTING CHAIN
NO
TRACE RESET CIRCUIT FROM A105-U14 PIN 3. REPLACE DEFECTIVE PARTS.
YES
CHECK A104
CONVERTER LOCK CKT

Figure 5-4. Non-Zero Display Test

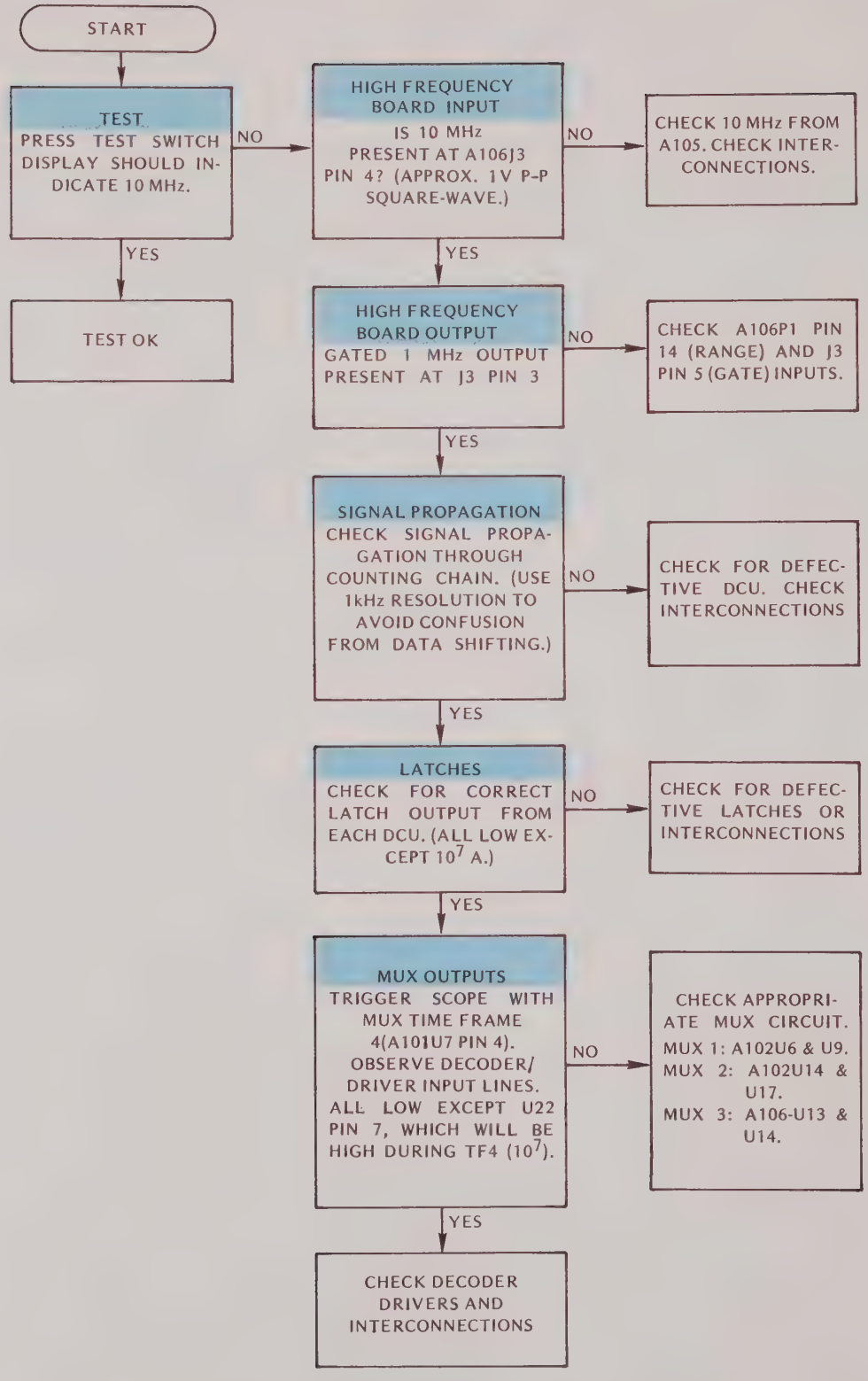

START
TEST
PRESS TEST SWITCH DISPLAY SHOULD INDICATE 10 MHz.
NO
YES
TEST OK
HIGH FREQUENCY BOARD INPUT
IS 10 MHz PRESENT AT A106J3 PIN 4? (APPROX. 1V P-P SQUARE-WAVE.)
NO
CHECK 10 MHz FROM A105. CHECK INTERCONNECTIONS.
YES
HIGH FREQUENCY BOARD OUTPUT
GATED 1 MHz OUTPUT PRESENT AT J3 PIN 3
NO
CHECK A106P1 PIN 14 (RANGE) AND J3 PIN 5 (GATE) INPUTS.
YES
SIGNAL PROPAGATION
CHECK SIGNAL PROPAGATION THROUGH COUNTING CHAIN. (USE 1kHz RESOLUTION TO AVOID CONFUSION FROM DATA SHIFTING.)
NO
CHECK FOR DEFECTIVE DCU. CHECK INTERCONNECTIONS
YES
LATCHES
CHECK FOR CORRECT LATCH OUTPUT FROM EACH DCU. (ALL LOW EXCEPT 10^7 A.)
NO
CHECK FOR DEFECTIVE LATCHES OR INTERCONNECTIONS
YES
MUX OUTPUTS
TRIGGER SCOPE WITH MUX TIME FRAME 4(A101U7 PIN 4). OBSERVE DECODER/ DRIVER INPUT LINES. ALL LOW EXCEPT U22 PIN 7, WHICH WILL BE HIGH DURING TF4 (10^7).
NO
CHECK APPROPRIATE MUX CIRCUIT.
MUX 1: A102U6 & U9.
MUX 2: A102U14 & U17.
MUX 3: A106-U13 & U14.
YES
CHECK DECODER DRIVERS AND INTERCONNECTIONS

Figure 5-5. Self-Test

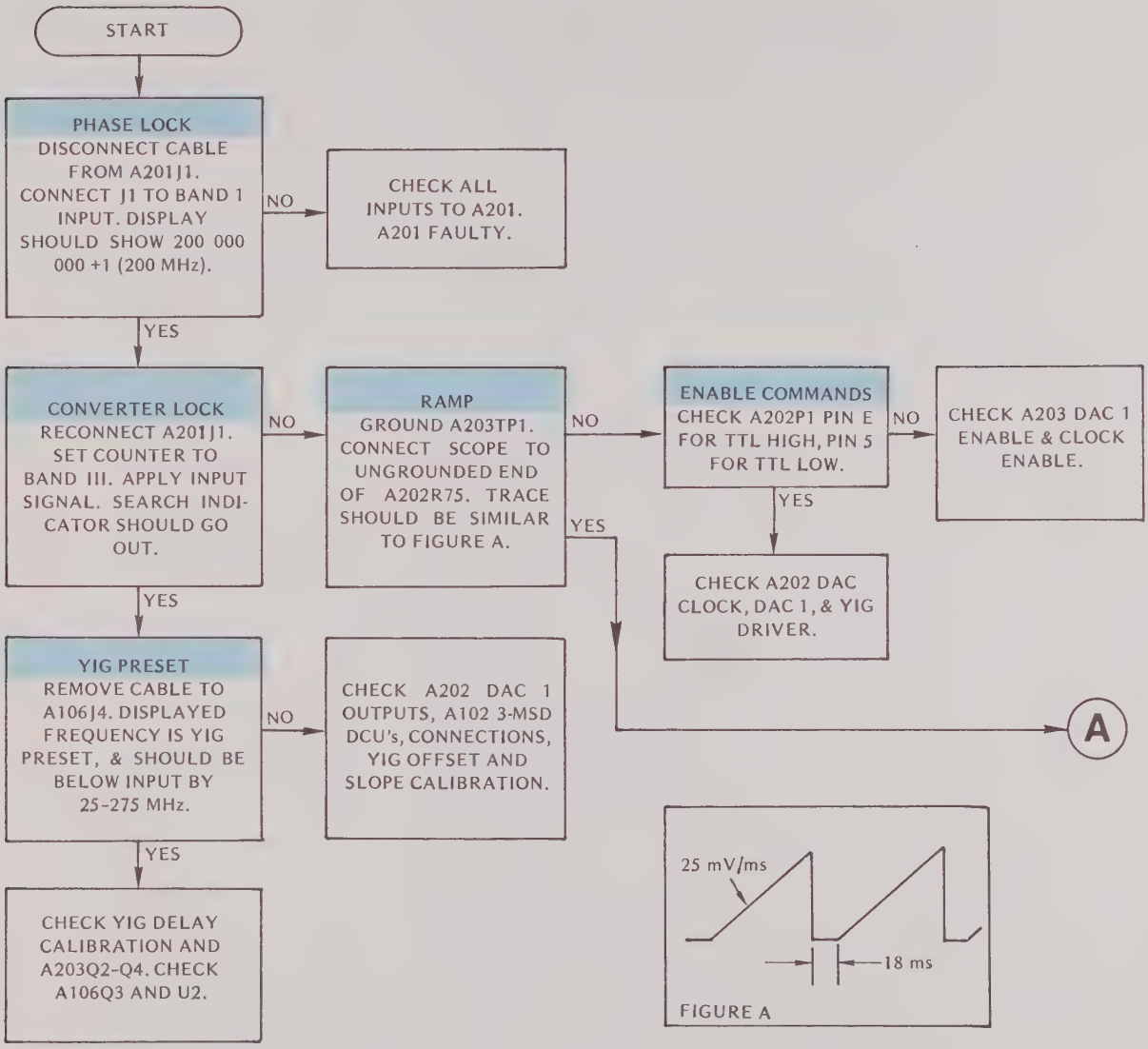

START
PHASE LOCK
DISCONNECT CABLE FROM A201J1. CONNECT J1 TO BAND 1 INPUT. DISPLAY SHOULD SHOW 200 000 000 +1 (200 MHz).
NO
CHECK ALL INPUTS TO A201. A201 FAULTY.
YES
CONVERTER LOCK
RECONNECT A201J1. SET COUNTER TO BAND III. APPLY INPUT SIGNAL. SEARCH INDICATOR SHOULD GO OUT.
NO
RAMP
GROUND A203TP1. CONNECT SCOPE TO UNGROUNDED END OF A202R75. TRACE SHOULD BE SIMILAR TO FIGURE A.
NO
ENABLE COMMANDS
CHECK A202P1 PIN E FOR TTL HIGH, PIN 5 FOR TTL LOW.
NO
CHECK A203 DAC 1 ENABLE & CLOCK ENABLE.
YES
CHECK A202 DAC CLOCK, DAC 1, & YIG DRIVER.
YES
A
YES
YIG PRESET
REMOVE CABLE TO A106J4. DISPLAYED FREQUENCY IS YIG PRESET, & SHOULD BE BELOW INPUT BY 25-275 MHz.
NO
CHECK A202 DAC 1 OUTPUTS, A102 3-MSD DCU's, CONNECTIONS, YIG OFFSET AND SLOPE CALIBRATION.
YES
CHECK YIG DELAY CALIBRATION AND A203Q2-Q4. CHECK A106Q3 AND U2.
25 mV/ms
18 ms
FIGURE A

Figure 5-6. Converter Troubleshooting

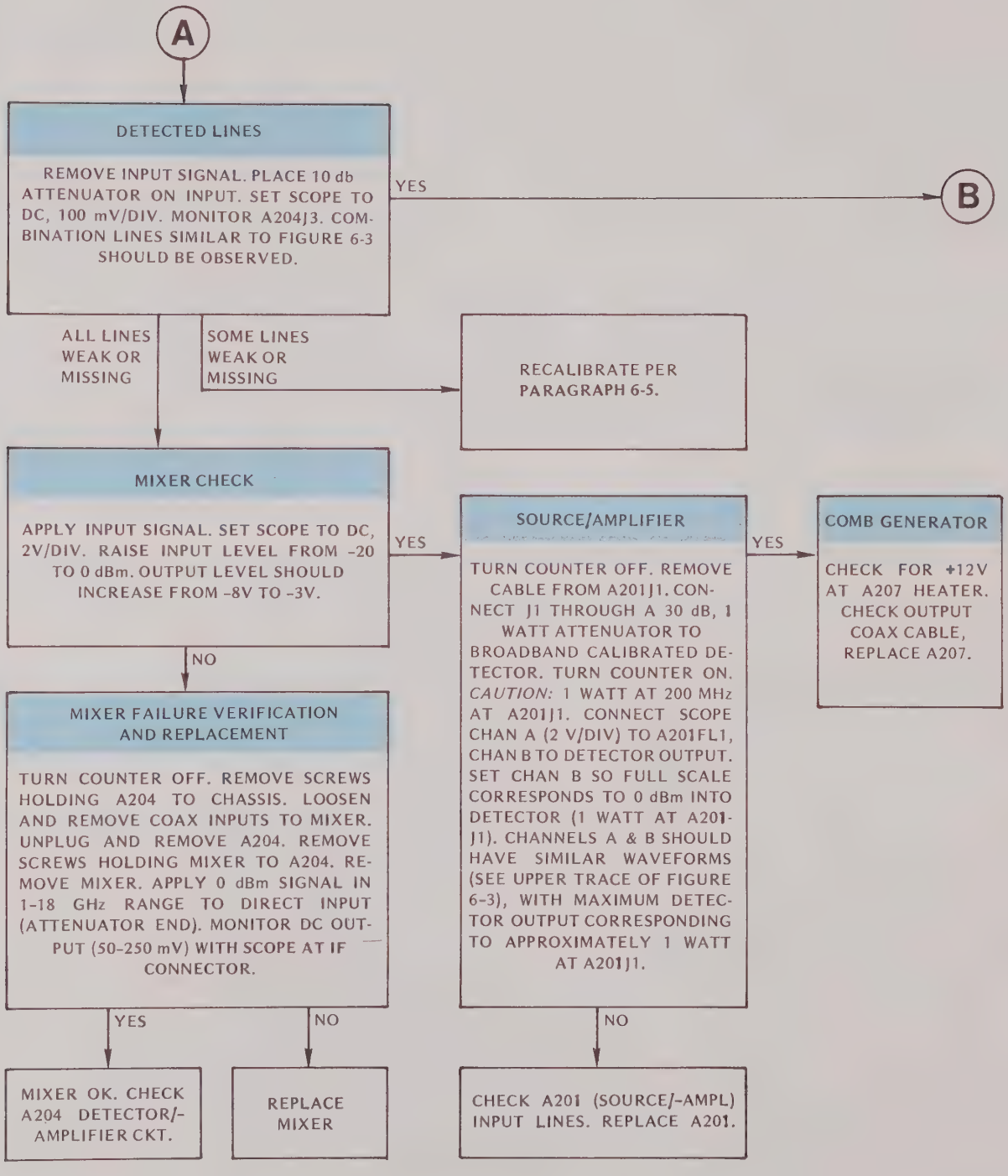

A
DETECTED LINES
REMOVE INPUT SIGNAL. PLACE 10 db ATTENUATOR ON INPUT. SET SCOPE TO DC, 100 mV/DIV. MONITOR A204J3. COMBINATION LINES SIMILAR TO FIGURE 6-3 SHOULD BE OBSERVED.
YES
B
ALL LINES WEAK OR MISSING
SOME LINES WEAK OR MISSING
RECALIBRATE PER PARAGRAPH 6-5.
MIXER CHECK
APPLY INPUT SIGNAL. SET SCOPE TO DC, 2V/DIV. RAISE INPUT LEVEL FROM -20 TO 0 dBm. OUTPUT LEVEL SHOULD INCREASE FROM -8V TO -3V.
YES
SOURCE/AMPLIFIER
TURN COUNTER OFF. REMOVE CABLE FROM A201J1. CONNECT J1 THROUGH A 30 dB, 1 WATT ATTENUATOR TO BROADBAND CALIBRATED DETECTOR. TURN COUNTER ON. CAUTION: 1 WATT AT 200 MHz AT A201J1. CONNECT SCOPE CHAN A (2 V/DIV) TO A201FL1, CHAN B TO DETECTOR OUTPUT. SET CHAN B SO FULL SCALE CORRESPONDS TO 0 dBm INTO DETECTOR (1 WATT AT A201-J1). CHANNELS A & B SHOULD HAVE SIMILAR WAVEFORMS (SEE UPPER TRACE OF FIGURE 6-3), WITH MAXIMUM DETECTOR OUTPUT CORRESPONDING TO APPROXIMATELY 1 WATT AT A201J1.
YES
COMB GENERATOR
CHECK FOR +12V AT A207 HEATER. CHECK OUTPUT COAX CABLE, REPLACE A207.
NO
MIXER FAILURE VERIFICATION AND REPLACEMENT
TURN COUNTER OFF. REMOVE SCREWS HOLDING A204 TO CHASSIS. LOOSEN AND REMOVE COAX INPUTS TO MIXER. UNPLUG AND REMOVE A204. REMOVE SCREWS HOLDING MIXER TO A204. REMOVE MIXER. APPLY 0 dBm SIGNAL IN 1-18 GHz RANGE TO DIRECT INPUT (ATTENUATOR END). MONITOR DC OUTPUT (50-250 mV) WITH SCOPE AT IF CONNECTOR.
YES
NO
NO
MIXER OK. CHECK A204 DETECTOR/-AMPLIFIER CKT.
REPLACE MIXER
CHECK A201 (SOURCE/-AMPL) INPUT LINES. REPLACE A201.

Figure 5-6. Converter Troubleshooting (Continued)

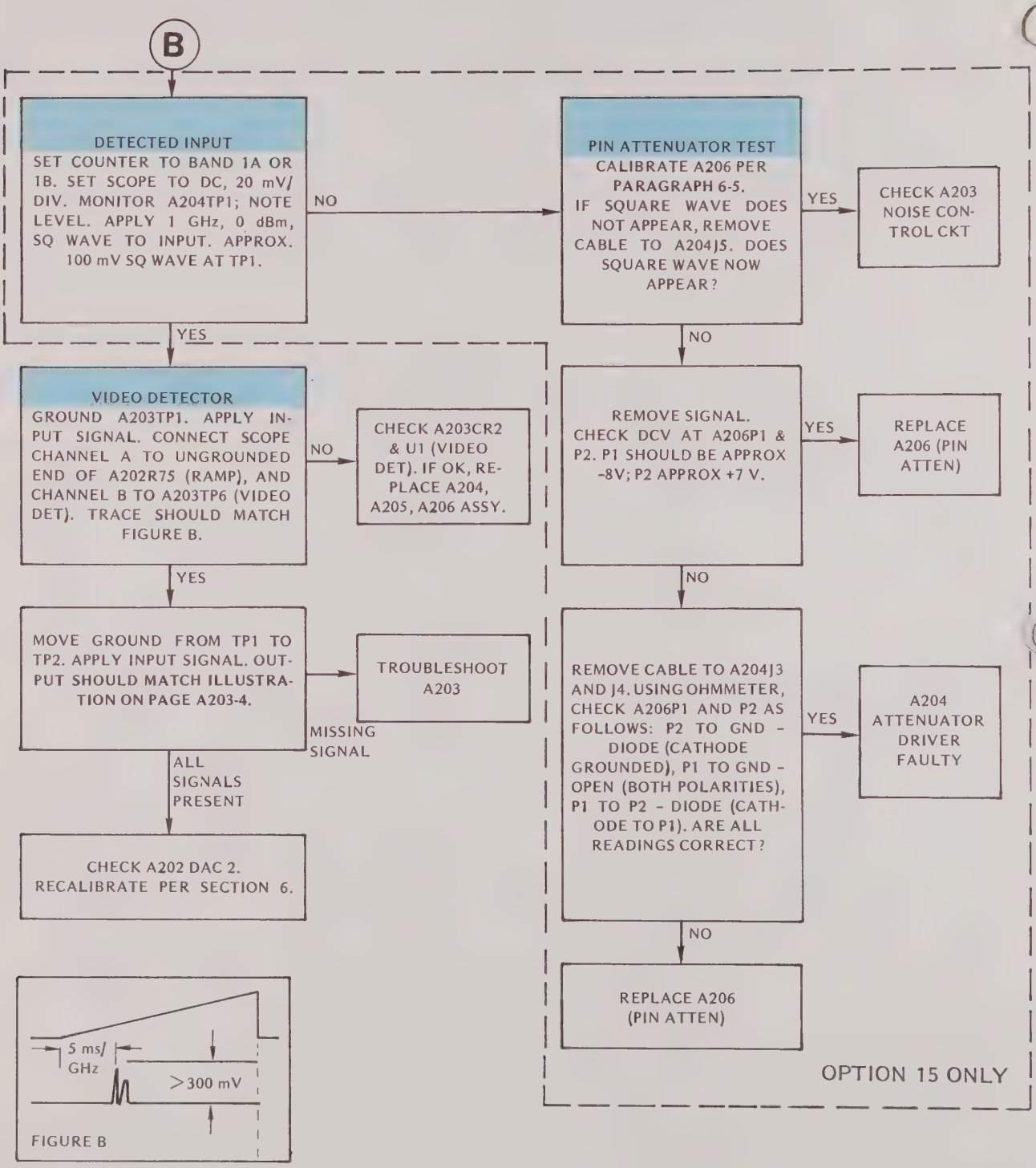

B
DETECTED INPUT
SET COUNTER TO BAND 1A OR 1B. SET SCOPE TO DC, 20 mV/ DIV. MONITOR A204TP1; NOTE LEVEL. APPLY 1 GHz, 0 dBm, SQ WAVE TO INPUT. APPROX. 100 mV SQ WAVE AT TP1.
NO
PIN ATTENUATOR TEST
CALIBRATE A206 PER PARAGRAPH 6-5.
IF SQUARE WAVE DOES NOT APPEAR, REMOVE CABLE TO A204J5. DOES SQUARE WAVE NOW APPEAR?
YES
CHECK A203 NOISE CONTROL CKT
YES
NO
VIDEO DETECTOR
GROUND A203TP1. APPLY INPUT SIGNAL. CONNECT SCOPE CHANNEL A TO UNGROUNDED END OF A202R75 (RAMP), AND CHANNEL B TO A203TP6 (VIDEO DET). TRACE SHOULD MATCH FIGURE B.
NO
CHECK A203CR2 & U1 (VIDEO DET). IF OK, REPLACE A204, A205, A206 ASSY.
REMOVE SIGNAL.
CHECK DCV AT A206P1 & P2. P1 SHOULD BE APPROX -8V; P2 APPROX +7 V.
YES
REPLACE A206 (PIN ATTEN)
YES
NO
MOVE GROUND FROM TP1 TO TP2. APPLY INPUT SIGNAL. OUTPUT SHOULD MATCH ILLUSTRATION ON PAGE A203-4.
TROUBLESHOOT A203
MISSING SIGNAL
ALL SIGNALS PRESENT
REMOVE CABLE TO A204J3 AND J4. USING OHMMETER, CHECK A206P1 AND P2 AS FOLLOWS: P2 TO GND - DIODE (CATHODE GROUNDED), P1 TO GND - OPEN (BOTH POLARITIES), P1 TO P2 - DIODE (CATHODE TO P1). ARE ALL READINGS CORRECT?
YES
A204 ATTENUATOR DRIVER FAULTY
NO
CHECK A202 DAC 2. RECALIBRATE PER SECTION 6.
REPLACE A206 (PIN ATTEN)
OPTION 15 ONLY
5 ms/ GHz
>300 mV
FIGURE B

Figure 5-6. Converter Troubleshooting (Continued)

Section 6
Adjustments and Calibration

6-1. GENERAL

Adjustments to the counter should be made only if the instrument is not operating within specifications, or following replacement of components. Test equipment required is specified in Table 5-1. If adjustments do not result in specified performance, refer to Section 5. Adjustment locations are shown in Figure 6-1.

CAUTION

It is essential that all adjustment procedures are performed in sequence.

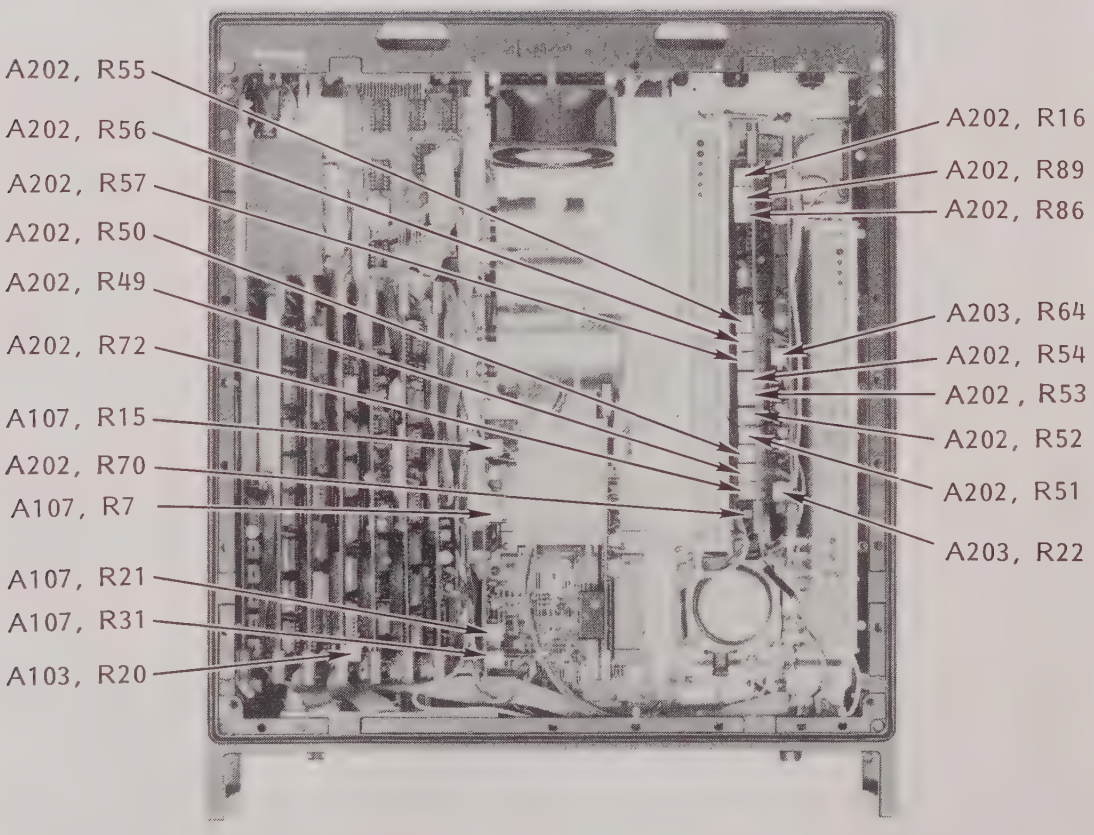


Figure 6-1. Calibration Adjustment Locator

6-2. POWER SUPPLY ADJUSTMENTS

Prior to power supply adjustments, warm up instrument for 20 minutes. All voltages are measured on the Counter Interconnect Board (A113).

1. Connect DVM to GND on A113.
2. Measure +12V output. Adjust A107R7 output to +12.000±.010V.
3. Measure +5V output. Adjust A107R15 output to +5.000±.010V.
4. Measure -12V output. Adjust A107R21 output to -12.000±.010V.
5. Measure -5.2V output. Adjust A107R31 output to -5.200±.010V.

6-3. VIDEO DETECTOR GAIN ADJUSTMENT

1. Disconnect cable from output of Video Amplifier (A204J2).
2. Connect a 150 MHz CW signal at -6 dBm to cable A203P2 (W21).
3. Connect DVM to Converter Control 1, Test Point A203TP6.
4. Adjust A203R41 for 340 ±20mV.
5. Reconnect cable to A204J2.

6-4. IN-BAND DETECTOR ADJUSTMENT

1. Disconnect cable from A204J2.

2. Connect sweep generator to A203P2. Set controls as follows:

   SWEEP . . . . . 265 MHz down to 235 MHz
   LEVEL . . . . . 0 dBm
   MARKERS . . . every 10 MHz

3. Connect dual trace oscilloscope as follows:

   HORIZONTAL . . . . . To sweep generator
   CHANNEL A . . . . . A203TP4 via vertical output on sweep generator

4. Adjust A203R21 so the switching spike is coincident with the 250 MHz marker as illustrated in Figure 6-2.

5. Reconnect cable to A204J2.

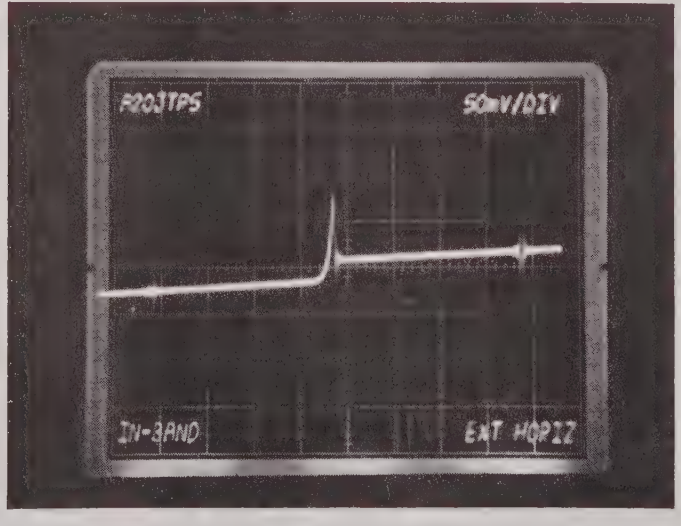


Figure 6-2. In-Band Detector Switching Point

6-5. COMB LEVELING, BIAS, AND THRESHOLD ADJUSTMENT

1. Unplug Source/Amplifier power plug A208J1.
2. Connect a 3 dB pad to the signal input connector. Apply a +3 dBm, 1.0 GHz, square-wave modulated signal to the pad.
3. Observe the square-wave signal at A204TP1.
4. Adjust A204R61 until the square-wave at TP1 is 90-100 mV in amplitude.
5. Reconnect Source/Amplifier power plug.
6. Connect dual trace oscilloscope as follows:
   CHANNEL A . . . . A204TP1 (Mixer Detected Output)
   CHANNEL B . . . . A201FL1 (Power Level Control)
   EXT. TRIG. . . . . A203TP8 (Converter Reset)
7. Set Channel A for DC coupling, 100mV/cm (standard) and 20mV/cm for Option 15. Set Channel B for DC coupling, 2V/cm.
8. Terminate signal input connector in 50 ohms (6 dB or greater, adequate).
9. Adjust potentiometers on Converter Control 2 (A202) so maximum comb line amplitude does not vary from levels specified in Table 6-1.
10. Remove 6 dB pad from input connector.

NOTE: Steps 1 through 5 apply to Option 15 only.

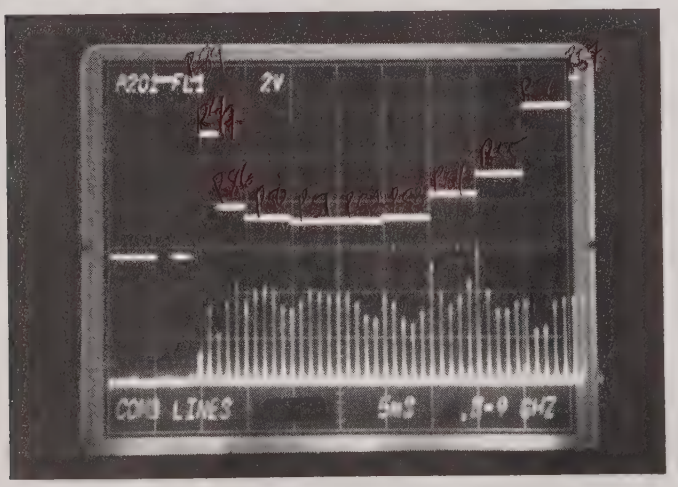


Figure 6-3. Typical Comb Level Adjustment

6-6. YIG DRIVER OFFSET AND SLOPE ADJUSTMENT

For this adjustment, a Summing Amplifier (capable of providing a variable DC offset) is recommended. One may be constructed as shown in Figure 5-1.

Alternatively, a dual trace oscilloscope with differential inputs (such as HP1200A) may be used. Apply a signal to one side of the differential input and a variable power supply to the other.

1. Connect dual trace oscilloscope as follows:

   CHANNEL A . . . . A203TP6 (Video Detector Output)
   CHANNEL B . . . . A202J3 pin 1 (Ramp) via Summing Amplifier
   EXT. TRIG. . . . . A203TP8 (Converter Reset)

2. Ground A203TP1.

3. Apply 1.1 GHz signal at -15 dBm to signal input.

4. Depress RESET switch.

5. With no DC offset applied, adjust Channel B vertical sensitivity so each ramp step is two vertical divisions (approximately 10 mV/div.). Set Channel A to 200 mV/div. Set time base to 5 ms/cm and set time base multiplier to X10. Oscilloscope display should appear as shown in Figure 6-4.

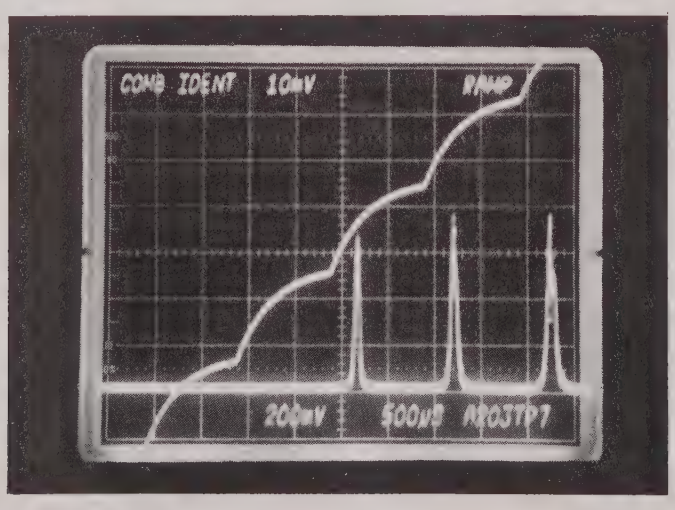


Figure 6-4. 1 GHz Comb Line Identification

6. Reduce the input frequency to 1.0 GHz. When the input frequency is exactly 1 GHz, the center line of the three comb lines on Channel A should null. This identifies the 1 GHz comb line. The 800 MHz comb line is the line preceeding the 1 GHz line.

7. Remove the ground from A203TP1 and place it on A203TP2. Depress the RESET switch.

8. Adjust YIG Offset A202R72 so the ramp resets at 50% (.8 div.) of the fourth ramp step (see Figure 6-5).

9. Tune slowly from 1 GHz to 18 GHz. As the frequency is changed, adjust the DC offset and the horizontal position control of the oscilloscope to maintain the upper portion of the ramp on the display. Above 10 GHz, the time base will need to be increased to 10 msec/div.

   As the frequency is changed, adjust YIG slope with A202R70, so the ramp reset occurs in the range of 40 to 60% of the full step amplitude. At 18 GHz, adjust R60 so reset occurs at 60% of the step amplitude.

10. Recheck YIG Offset A202R72 and readjust at 1 GHz if necessary. If A202R72 is re-adjusted, it will be necessary to reset YIG Slope A202R70 at 18 GHz.

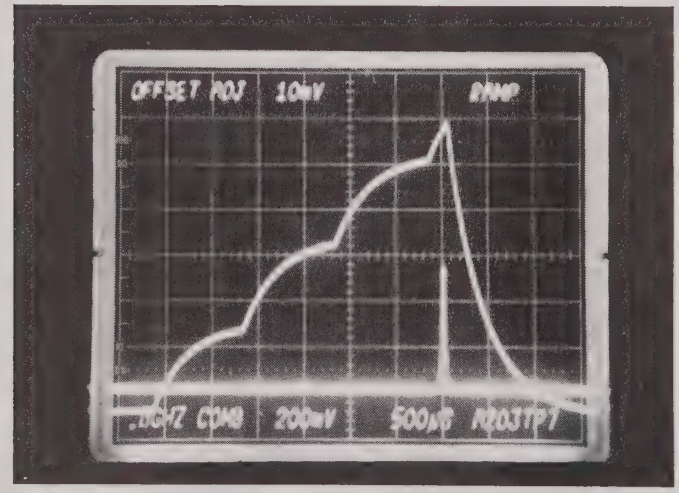


Figure 6-5. YIG Driver Offset Adjustment

6-7. YIG DELAY CORRECTION

1. With connections as in paragraph 6-6, set input frequency to 1 GHz at -15 dBm, and oscilloscope time base control to 10 ms/div., unexpanded.

2. Adjust YIG Delay Correction A202R4 so display appears approximately as shown in Figure 6-6.

3. Set Time Base to variable (approximately 5 ms/div.) and externally trigger oscilloscope from A203P1 pin 12 (DAC 2 ENABLE). Adjust oscilloscope time base so DAC 2 ramp occupies the full screen.

4. Adjust A202R16 so the 50% point of the leading edge of the video pulse occurs one division to the right of center of the DAC 2 ramp as shown in Figure 6-7. Note that the point marked "Ramp Start" is 3 ms after DAC 2 ENABLE, and that the point marked "Ramp Center" is *not* the center of the display.

5. Tune to 18 GHz and observe position of leading edge with respect to DAC 2 "Ramp Center." This should be approximately one division to the left of "Ramp Center."

6. If necessary readjust A202R16 until the leading edge of the video pulse is the same distance to the right of "Ramp Center" at 1 GHz, as it is to the left of "Ramp Center" at 18 GHz.

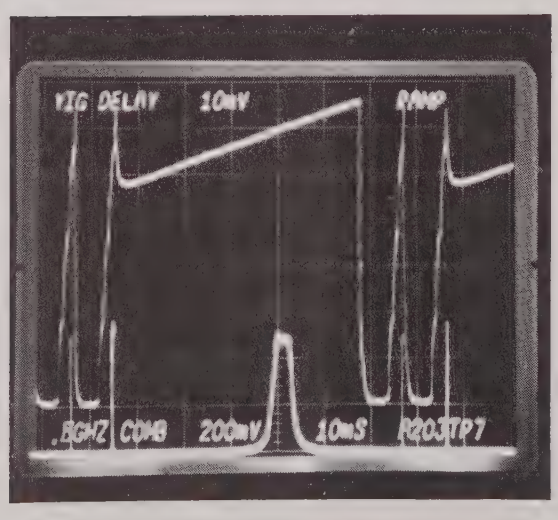


Figure 6-6. YIG Delay Correction 1

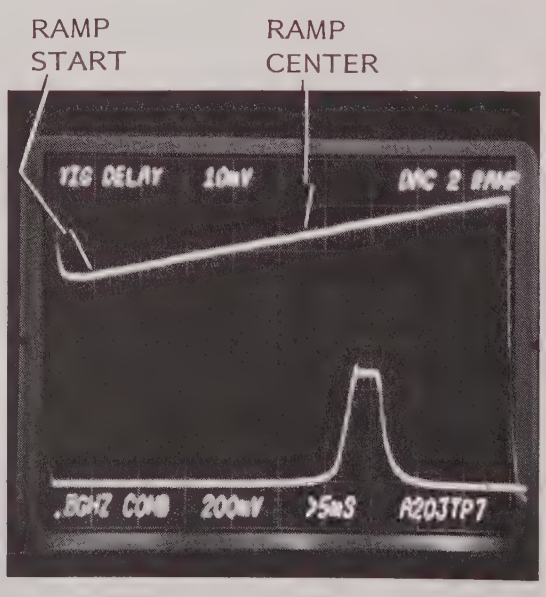


Figure 6-7. YIG Delay Correction 2

6-8. OPTIONAL VIDEO DETECTOR GAIN ADJUSTMENT

When optimum sensitivity is required, this procedure should be performed in addition to the procedure in paragraph 6-3.

A stable source is required that is within the frequency range of the counter, and has variable output power. Short term stability should be 1 kHz or better.

1. Set source power level to -20 dBm.

2. Observe frequency indication.

3. Reduce input power slowly while frequently pressing the RESET switch. At some power level the counter will fail to lock.

4. Increase power slightly so that counter just achieves LOCK and a frequency is displayed.

5. Displayed frequency should be correct (no reduction in frequency). Increase Video Detector gain (adjust A203R41), and repeat steps 3. and 4. until an erroneous count is obtained.

6. Once an erroneous count is obtained, begin decreasing Video Detector gain and repeat steps 3. and 4. until frequency indication is either correct or zero (no LOCK) as power level is varied and counter is reset.

6-9. FINAL COMB LEVELING/BIAS

The most important function of comb leveling is to insure that spurious mixing products (resulting from doubling the comb frequency within the Mixer), do not cause erroneous readings, and that maximum output is below the lock threshold.

1. Connect oscilloscope as follows:

   CHANNEL A . . . . A203TP6 (Video Detector Output)

   CHANNEL B . . . . A201FL1 (Power Level Control)

   EXT. TRIG. . . . . A202P1 pin 12 (Converter Reset)

   TIME BASE . . . . 2 ms/div.

2. Ground A203TP1.

3. Apply a 1.5 GHz signal at +7 dBm and observe the Video Detector Signal.

4. Slowly tune the frequency upward. At some frequencies a spurious output, corresponding to approximately one-half the input frequency, will be visible.

5. While varying the frequency from 1.5 to 18 GHz, adjust the controls (listed in Table 6-1) so no spurious signal exceeds 300 mV amplitude. Vary oscilloscope time base setting as required to keep the display on the screen. A typical display is shown in Figure 6-8.

CAUTION

Do not attenuate comb lines more than absolutely necessary to maintain maximum spurious outputs of 300 mV. Comb line power relates directly to sensitivity.

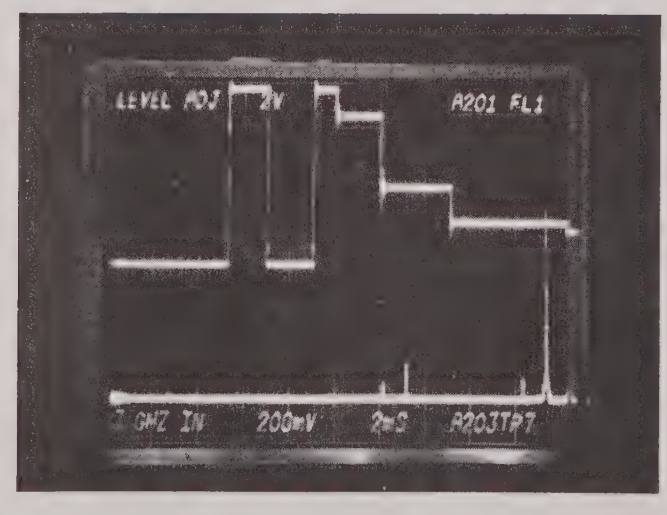


Figure 6-8. COMB Frequency Harmonic Generation

Table 6-1. COMB Level Adjustments

ADJUSTMENT	COMB LINE AFFECTED (GHz)	NOMINAL MAXIMUM LEVEL 350D	351D
A202R49	1.0, 1.2	300 mV	300 mV
A202R86	1.4, 1.6, 1.8	300 mV	300 mV
A202R50	2.0, 2.2, 2.4, 2.6, 2.8	300 mV	300 mV
A202R51	3.0, 3.2, 3.4, 3.6, 3.8	300 mV	300 mV
A202R52	4.0, 4.2, 4.4, 4.6, 4.8	300 mV	300 mV
A202R53	5.0, 5.2, 5.4, 5.6, 5.8	300 mV	300 mV
A202R54	6.0, 6.2, 6.4, 6.6, 6.8	300 mV *	300 mV
A202R55	7.0, 7.2, 7.4, 7.6, 7.8	No Max	300 mV
A202R56	8.0, 8.2, 8.4, 8.6, 8.8	No Max	300 mV
A202R57	9.0, 9.2, 9.4, 9.6, 9.8	No Max	300 mV * *

* 6.0 and 6.2 GHz only * * 9.0 GHz only

NOTE: Additional leveling (if required) obtained by selective addition of R83-96 and R112-121.

6-10. TIME BASE CALIBRATION

It is important to note that the precision of the time base calibration directly affects overall counter accuracy. Reasons for recalibration, and the procedures to be used, should be thoroughly understood before attempting any readjustment.

The fractional error in the frequency indicated by the counter, is equal to the negative of the fractional frequency error of the Time Base Oscillator with respect to its true value. That is:

$$\frac{\triangle f_s}{f_s} = -\frac{\triangle f_t}{f_t}$$

where f_s is the true frequency of the measured signal, and f_t is the true frequency of the Time Base Oscillator. Thus, the inaccuracy associated with a frequency measurement is directly related to the quality of the Time Base Oscillator, and a measure of the precision with which it was originally adjusted.

6-11. TEMPERATURE COMPENSATED CRYSTAL OSCILLATOR (TCXO) CALIBRATION

The standard Time Base Oscillator used in the counter is a TCXO (A116). The range of the actual measured frequencies of this oscillator will differ by no more than 2 parts in 10^6 if the temperature is slowly varied from 0 to +50 degrees C.

With a stable input frequency, the measurement indicated by the counter will fluctuate proportionally to the TCXO drift. To center this fluctuation on the true value of the measured signal, each TCXO has imprinted on its side the frequency setting required at +25 degrees C.

At approximate room temperature (+25 degrees C.), the slope of the frequency vs. temperature curve is normally no worse than -1×10^{-7} parts per degree C. When the counter is used in an ordinary laboratory environment, the TCXO may be set as close to 10000000 Hz as desired. In this environment, a peak-to-peak temperature variation of 5 degrees C. will result in a measured signal error of no more than $\pm 2.5 \times 10^{-7}$ parts. This signal error is due to the temperature characteristics of the Time Base Oscillator.

The natural aging characteristics of the crystal in the Time Base Oscillator can also cause inaccurate signal measurements. Aging refers to the long term, irreversible change in frequency (generally in the positive direction) which all quartz oscillators experience. The magnitude of this frequency fluctuation in the TCXO is less than 3×10^{-7} parts per month as specified. This may improve to at least 1×10^{-6} parts per year when in continuous operation.

Error due to aging adds directly to error due to temperature. The number of times the counter requires recalibration depends on the environment in which the counter operates, and upon the level of accuracy required.

For example, if the counter is subjected to the full operating temperature range one month after proper initial adjustments, the inaccuracy could vary from $+1.3 \times 10^{-6}$ parts to -0.7×10^{-6} parts.

CALIBRATION PROCEDURE:

1. Remove top cover of counter. Connect counter to reliable power source. Note ambient temperature.

2. Measure the frequency of the TCXO at the rear panel 10 MHz connector, with a second counter of known calibration accuracy.

3. Adjust the TCXO by turning the calibration screw on the TCXO case until the measured frequency equals that shown on the TCXO calibration label.

4. TCXO calibration is complete.

6-12. RANGE AND SENSITIVITY PERFORMANCE TEST

During this test connect the counter to the power source through a variable voltage device (see Table 5-1), so that line voltage may be varied ±10% from nominal (115 or 230 Vac).

1. Set SAMPLE RATE fully counter-clockwise.

2. Connect leveled source output to signal input.

3. Vary signal frequency from 825 MHz to 18 GHz at levels:

   825 MHz to 1.1 GHz at -15 dBm (40 mV rms)

   1.1 GHz to 12.4 GHz at -20 dBm (22 mV rms)

   12.4 GHz to 18.0 GHz at -15 dBm (40 mV rms)

The counter should now display correct input frequency.

Section 7
Functional Description and Illustrated Parts Breakdown

This section contains a functional description, a parts list, an illustration and a schematic diagram for each printed circuit board used in this counter.

The parts list is broken down by types of components, listed in alphanumeric sequence. The components that have a different reference designator (REF DES), but have the same EIP part number, are described for the first such component listed. Subsequent descriptions of that component will refer to the first entry. The total number of like components used on the same assembly will be listed with the first entry in the column identified as UNITS PER ASSY.

The last two columns of the parts list will supply the name of the manufacturer and their Federal Supply Code for Manufacturers (FSCM) number. A list of manufacturers names, addresses and their Federal Supply Code for Manufacturers (FSCM) number are given in Appendix A. The FSCM number is used in the parts list as a guide to the manufacturer or supplier of a part.

7-1. REFERENCE DESIGNATORS

A	Assembly
B	Battery or Fan
C	Capacitor
CR	Diode
DS	Indicator (display)
F	Fuse
J	Jack or Connector
K	Relay
L	Inductor
P	Plug or PCB contacts
Q	Transistor
R	Resistor
S	Switch
T	Transformer
TP	Test Point
U	Integrated Circuit
W	Wire (cable)
X	Socket or Holder
Q1-3	Q1 *through* Q3
Q1/2	Q1 *and* Q2 (matched pair)

7-2. ABBREVIATIONS

CAP	Capacitor
CBN	Carbon
CER	Ceramic
CMT	Cermet
CNTR	Counter
CONV	Converter
COMP	Composition
CONN	Connector
DI	Diode
ELEC	Electrolytic
FDTH	Feedthrough
FLM	Film
FML	Female
GP	General Purpose
IC	Integrated Circuit
K	Kilo (x 1,000)
LED	Light-emitting-diode
M	Meg (x 1,000,000)
MET OX	Metal Oxide
MF	Metal Film
MH	Millihenry
ML	Male
MTCH PR	Matched Pair
PC	Printed Circuit
PCB	PC Board Assembly
PF	Picofarad
PREC	Precision
RSTR	Resistor
RT AN	Right Angle
S.A.T.	Value or type selected during factory test. Part may not be used.
SW	Switch
TANT	Tantalum
TRIM	Trimmer
UF	Microfarad
UH	Microhenry
VAR	Variable
WPRF	Waterproof
WW	Wirewound
XSTR	Transistor

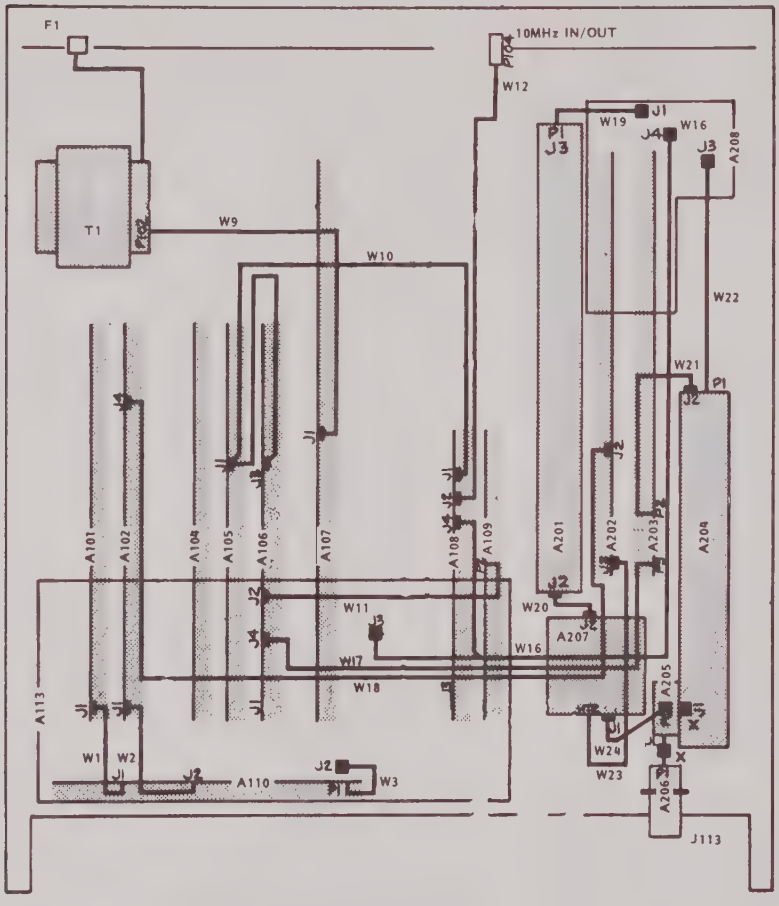
7-3. MODEL 331 COUNTER (TOP ASSEMBLY) PARTS LIST

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A1	Counter, 331			EIP Microwave	
B1	Fan, Axial, 115 Vac	5000151	1	8500	23936
F1	Fuse, 1.5A, SB, 3AG, 115V	5000101	1	MDX-1-1/2	74100
F	Fuse, .75A, SB, 3AG, 230V	5000079	1	MDL-3/4A	74100
J1	Pwr Recpt	2640005	1	EAC-301	82389
J2	Option 39, conn, 50 pin	2640004	1	57-40500	02660
J3	Option 31, 36, conn, 50 pin	2640004	1	"	"
J4	10 MHz, conn, BNC	2610024	1	KC-79-35	91836
J113	P/O A206				
	Smpl RT Knob	5000056			
	Tilt Bail	5000055			
	Top Cover	5210023			
	Bottom Cover	5210024			
	MTG Foot	5220002			
	AC Pwr Cord	5440002			
S1	Switch, Pwr	4500008			
S102	Switch, 115/230V	4520006			
T1	Pwr Transformer	4900004			
XF1	Fuse Holder	5000052			
	PCB ASSEMBLIES			SEE PAGE NO.	
A101	Count Chain 1	2020036	1	101-1	
A102	Count Chain 2	2020034	1	102-1	
A104	Control 2	2020010	1	104-1	
A105	Control 1	2020009	1	105-1	
A106	High Frequency	2020120	1	106-1	
A107	Power Supply	2020077	1	107-1	
A108	Reference Osc Buffer	2020012	1	108-1	
A110	Display (31)	2020004	1	110-1	
A113	Counter Interconnect	2020122	1	113-1	
A116	TCXO	2030002	1	no replaceable pts	
A2	Converter Tray A2Q1	4710009	1		
A201	Source Amplifier	2020091	1	201-1	
A202	Converter Control 2	2020067	1	202-1	
A203	Converter Control 1	2020066	1	203-1	
A204	Video Amplifier (P/O 2010061)	2010014	1	204-1	
A205	Mixer	2010007	1	205-1	

7-3. MODEL 331 COUNTER (TOP ASSEMBLY) PARTS LIST (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A206	Pin Diode Attenuator OP 15	2010061	1	206-1	
A207	YIG Comb Generator	2010097	1		
A208	Converter Interconnect	2020044	1		
	J1	2620042	1		
	J2	2040027	1		
	J3	2620014	1		

7-4. ASSEMBLY LOCATIONS AND CABLE INTERCONNECTIONS



CABLE INTERCONNECTION GUIDE

BASIC COUNTER

FROM	CABLE	TO
A110-J1	W1	A101-J1
A110-J2	W2	A102-J1
A110-P1	W3	A113-J2
A111-P1	W4	A113-J4
J111	X	A111-J1
A111-J2	W5	A106-J1
S2	W6	A113-J6
J112	W7	A109-J1
REAR PNL	W8	J101
P102 (T1)	W9	A107-J1
A108-J1	W10	A105-J1
A106-J3		A103-J2
A109-P2	W11	A106-J2
P104	W12	A108-J2
P103	W13	A113-J5
A108-J3	W14	A112-J1
P101	W15	A114 (T2)

CONVERTER

FROM	CABLE	TO
A208-J2	W16	A113-J3
		A108-J4
A203-P3	W17	A106-J4
A202-J2	W18	A102-J4
A201-P1	W19	A208-J1
A201-J1	W20	A207-J2
A203-P2	W21	A204-J2
A204-P1	W22	A208-J3
A202-J3	W23	A207-HTR
		A2-Q1
A205-P1	W24	A207-J1
A205-P2	X	A204-J1
A205-J1	X	A206-P1

LEGEND:

- X — Direct-Coupled (no cable assy)
- Cable - to - Assembly
- Cable - to - Assembly
- Cable - to - Cable

CABLES SHOWN ARE FOR STANDARD 350D & 351D. A112, A114 TYPICAL FOR OPTIONS 03, 04, 05.

CAUTION: Use care when plugging in 14 pin ribbon cable connectors: W1, W2, W10, and W18. Use removal tool (EIP Part 5000094) for extraction.

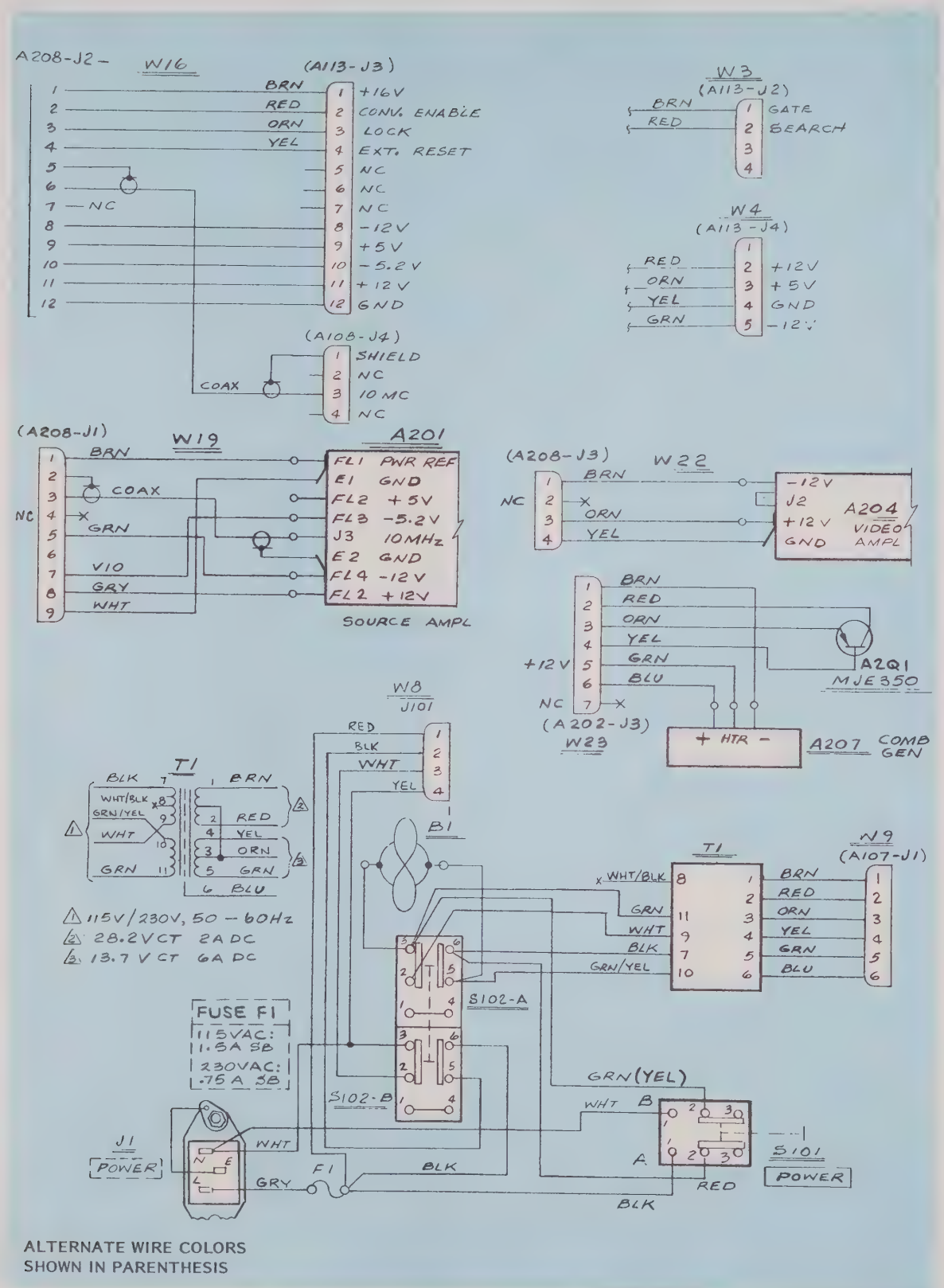


Figure 7-1. 331 Counter Interconnection Diagram

7-5. INTRODUCTION TO COUNT CHAINS 1, 2 AND 3

Count Chain Boards 1, 2, and 3 perform most of the actual frequency counting functions of the direct counter. The main components are the Count Chain, the Storage Unit, and the Display Multiplexer.

The Count Chain consists of a string of 8 cascaded decimal counting units (DCU's). The first DCU (on the High Frequency Board A106) must be fast enough to count the 300 MHz direct input. The second DCU (on A103) must follow the 30 MHz output of the first.

The remaining DCU's (on A103) are standard TTL integrated circuits.

The storage unit is a string of quad latches for each of the eight DCU's of the count chain. An enable signal (update data) to the storage unit causes it to load the information from the count chain.

The display multiplexer processes the information held in the storage unit. The output of the storage unit is converted to the seven line code needed to drive the seven segments of each display digit. Power is applied to each digit sequentially for 25% of the time.

PHYSICAL ORGANIZATION

The count chain is divided among A102, A103, and A106 as follows:

- A106 contains the first DCU.
- A103 contains the second DCU, the latch for the first DCU, and the multiplexer for the first DCU.
- A102 contains the remaining 6 DCU's, the last 7 latches, and 2 multiplexers. Two decoders convert the multiplex output to the 7 line code to drive the first 4 digits.

Board A101 includes the third decoder-driver for the last 4 digits, buffer circuits for the front panel resolution switches, timing circuits for the multiplexer and display, and leading zero suppression circuitry.

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A101
COUNT CHAIN 1

Count Chain 1 (A101) generates the correct timing sequence and control commands for the multiplex system, provides leading zero blanking of the display, and controls shifting of data from DCU to DCU in the counting chain in response to changes in gate time length.

In addition, A101 accepts the inputs from the front panel RESOLUTION switches, and processes them into control signals for the multiplex system and the Time Base Generator on Control 1 (A105). A101 also contains the third decoder driver for the display.

MULTIPLEX SYSTEM OPERATION

The multiplex system is composed of three individual multiplex channels designated MUX 1, MUX 2, and MUX 3. Each MUX channel includes a four-to-seven line decoder-driver which drives segments of the front panel display. MUX 1 controls the four most-significant digits of the display (10 GHz, 1GHz, 100 MHz and 10 MHz). MUX 2 controls the middle three digits and MUX 3 the least-significant digits. The input information for MUX 1, 2, and 3 is obtained from the eight quadlatch units on Count Chains 2 and 3 (A102 and A103).

So each multiplex circuit and decoder will be able to drive four digits, the multiplex timing sequence is broken down into four intervals designated Time Frames 1 through 4 (TF1 - TF4). Only one display digit in each channel is illuminated in a given Time Frame, as determined by the display digit selectors. The actual number displayed by the selected digit is determined by segment drive from the decoder-driver which drives all corresponding segments in that channel in parallel. If one of the selected digits is not to be illuminated, its segment drive is canceled by a blanking signal to the appropriate decoder-driver.

The three least significant digits may be blanked by depressing the appropriate RESOLUTION switches. The gate time remains at 1 ms in these positions.

The MUX timing sequence is actually three groups of four time frames. The first two groups occur at a rate of 2.5 MHz, the last at 25 kHz. The fast groups are used only to gather zero suppression information. Display occurs only during the slow group.

MULTIPLEX SEQUENCE GENERATOR

Clock pulses for the multiplexer are obtained from a 2.5 MHz clock signal derived from the 10 MHz Time Base Oscillator (A116). This signal is processed through a circuit composed of DCUs U1 and U5, ÷ 16 U2, the inverters of U6, and the gates of U11. The "SET 9" inputs of the DCUs are tied together, so that applying a high level to this input causes the 2.5 MHz clock to be fed through the gates to U2 at a 2.5 MHz rate.

With a low "SET 9" the input to U2 is one-hundredth the 2.5 MHz rate, or 25 kHz. The "SET 9" inputs to U1 and U5 are the inverted D output from U2, which is high when U2 is reset. The clock to U2 is then at a 2.5 MHz rate for eight pulses after reset. The D output then switches, and the clock rate drops to 25 kHz for the next four pulses. The A and B outputs of U2, plus their complements, are combined in the four NOR gates of U7 to produce the four MUX timing signals TF1, TF2, TF3, and TF4. The output TF4 is combined with U2 output D, and applied to the J input of flip-flop U23B. The clock to U23 and U24 is the same as the input to U2. The end of the fourth slow clock pulse then triggers U23B which resets U2. The clock pulses then return to the 2.5 MHz rate. The next pulse resets U23B and returns U1, U2, and U5 to their initial states.

The result is to produce a frame consisting of eight MUX time intervals at the 2.5 MHz rate, followed by four at the 25 kHz rate. One extra clock pulse resets the generator. The drive to the front panel display from U10 is gated off by the D output of U2 during the eight fast pulses in this train.

DISPLAY SELECTOR DRIVE GENERATOR

This drive is actually the same as the MUX Time Frame signals during the slow scan. The signals TF1 – TF4 provide one input to each of the four NAND gates of U10. The other four inputs are tied together with the D output of U2. This D output is high only after the first eight fast scan signals (first two groups of TF1 – TF4) have occurred, and the slow scan (third group of TF1 – TF4) is taking place. The NAND gate outputs are the inputs to the digit selector drivers on Display Board (A110).

SIGNAL GENERATORS FOR BLANKING

These generators operate on the inputs from the 3 front panel RESOLUTION switches. They are processed in the inverters of U4 and U8, and the NOR gates of U3 and U12, to produce nine output control signals. Five of these are used on A101 principally to control display blanking. The remaining four are used externally, as well as on A101. The four lines, one of which is high for each gate time, are fed to the line generator on A105, which then determines the gate time. One of these four signals, plus the remaining five, are used on A101 to control least significant digit blanking by the RESOLUTION switches. Three outputs of U20 produce blanking signals in Display Driver 2, by combining MUX timing outputs TF2, TF3, and TF4 with the RESOLUTION switch signals from U4 and U8. This produces blanking in readout digit 7 plus blanking of digits 5 and 6 in resolution settings for 100 kHz and 1 MHz. U17 produces the blanking signals in Display Drive 3 plus complete blanking (TF1 – TF4) in the 100 kHz and 1 MHz resolution settings. In the 331 the 1 kHz resolution switch is grounded, forcing the counter to always be in the 1 ms time base, and only allowing blanking down to 1 kHz.

LEADING ZERO SUPPRESSION CIRCUITRY

The portion of A101 related to leading zero suppression is detailed in Figure 101a. This function is accomplished in two steps. Initially, the circuit determines if any of the three channels contain non-zero data. If all data is zero, it disables the blanking and displays all zeros. If there is non-zero data, it locates the first channel containing this data.

The most vital portion of the zero suppression circuitry is contained within the decoder-drivers themselves. This is a zero detection circuit which is enabled by the ripple blanking input (RBI). If RBI is enabled (low), the presence of zero data causes the ripple blanking output (RBO) to be energized (low). The decoder-driver also contains a blanking input (BI) which blanks the digit when energized (low). BI and RBO are internally tied together so that the pin designated BI/RBO serves both as an input and an output. Thus, if RBI is enabled, zero data will energize RBO, which is equivalent to energizing BI, and the digit is blanked. Thus, a digit may be blanked either by applying a low-level to BI/RBO, or by the presence of zero data when RBI is enabled.

The first circuit function determines if any of the three channels contain non-zero data. All flip-flops are reset enabling the RBI on all decoder-drivers. As the multiplex system rapidly scans through its first four Time Frames, any non-zero data in a decoder-driver will be indicated by the RBO going high. This in turn enables the J input of the corresponding flip-flop. The next timing pulse sets that flip-flop and disables the RBI of that decoder-driver. At the end of the first multiplex group, the presence of any non-zero data is indicated by a set flip-flop. A set flip-flop enables the J input of the following flip-flop. This insures that non-zero data in any decoder-driver causes all flip-flops further down the chain to be set within two additional Time Frames.

If all data is zero, then the gating will allow the eight clock pulse (TF4 of the second fast group) to set the first two flip-flops and enable the third. The ninth clock pulse then sets the third flip-flop. This disables all ripple blanking inputs so no blanking will occur with all zero data.

The remaining task is to identify the first channel with non-zero data. Gates are arranged so that the ninth clock pulse will reset the first flip-flop which is in the "set" state via the K input, and thus enable the coresponding RBI, prior to the start of the slow scan. The internal ripple blanking circuitry will then blank all zeros until the first non-zero data is present.

A101 Count Chain 1

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A101-	Count Chain 1	2020036	1		
C1	Cer, .01uF, 20%, 100V	2150003	8	TG-S10	56289
C2	Tant, 33uF, 10V	2300015	1	TAG-20-33/10-50	14433
C3	C1				
C4	C1				
C5	Mica, 220pF, 5%, 500V	2250011	3	DM15CD221JO	72136
C6 thru C10	C1				
C11	C5				
C12	C5				
J1	14 Pin, Nylon	2630003	1	A-4497-14	0000A
R1 thru R6	Comp, 3.3K ohms, 5%	4010332	6	RCO7GF332J	81349
R7	Comp, 390 ohms, 5%	4010391	2	RCO7GF391J	81349
R8					
R11	Comp, 1.2K ohms, 5%	4010122	6	RCO7GF122J	81349
R12	Comp, 2.2K ohms, 5%	4010222	1	RCO7GF222J	81349
R13	R8				
R14	R8				
R15 thru R21	Comp, 100 ohms, 5%	4010101	7	RCO7GF101J	81349
R22	R7				
U1	Decade Counter	3087490	3	DM74LS90	0000X
U2	4 Bit Binary Counter	3087493	1	DM74LS93	0000X
U3	Quad, 2INP, NOR Gate	3087402	5	DM74LS02	0000X
U4	Hex Inverter	3087404	4	DM74LS04	0000X
U5	U1				
U6	U4				
U7	U3				
U8	U4				
U9	U1				
U10	Quad, 2INP, NAND Gate	3087401	1	DM74LS01	0000X
U11	Tri, 3INP, AND Gate	3087411	1	DM74LS11	0000X
U12	U3				
U13	Quad, 2INP, AND Gate	3087408	1	DM74LS08	0000X
U14	U3				

A101 Count Chain 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U15	Preset DEC Counter	3074167	1	DM74176N	0000X
U16	U4				
U17	4 Wide, 2INP, A01 Gate	3007454	1	DM7454	0000X
U18	Quad, 2INP, NAND Gate	3087400	2	DM74LS00	0000X
U19	U3				
U20		3087403	1	DM74LS03	0000X
U21	Hex Inverter	3087405	1	DM74LS05	0000X
U22	BCD, 7 Seg Decoder	3087447	1	DM74LS47	0000X
U23	Dual J-K FF	3087476	2	DM74LS76	0000X
U24	U23				

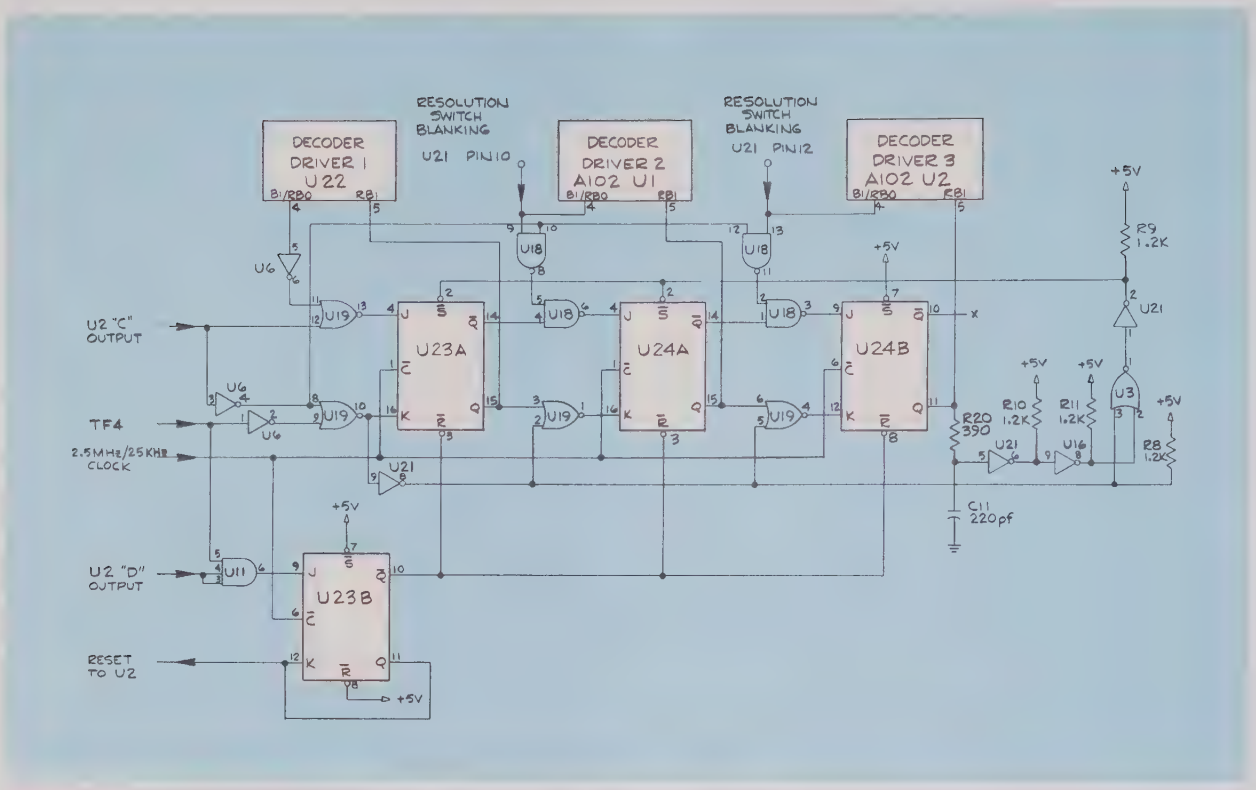
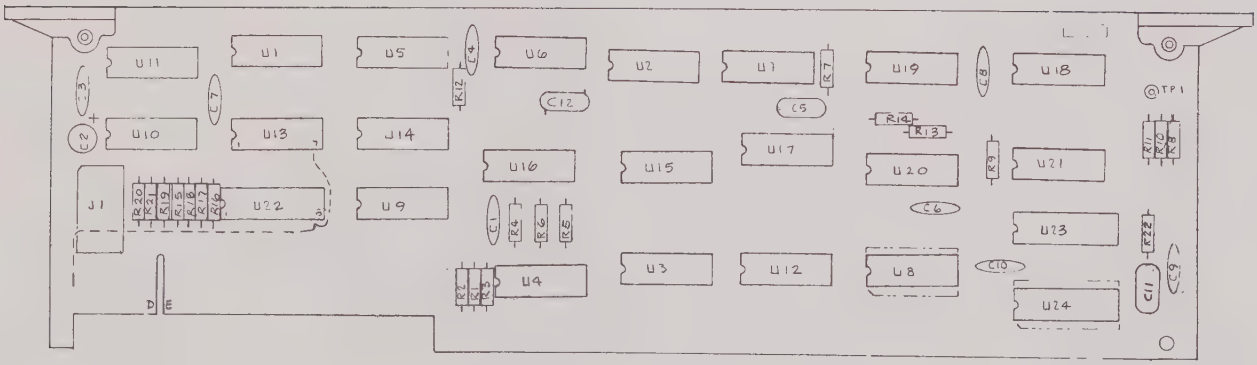
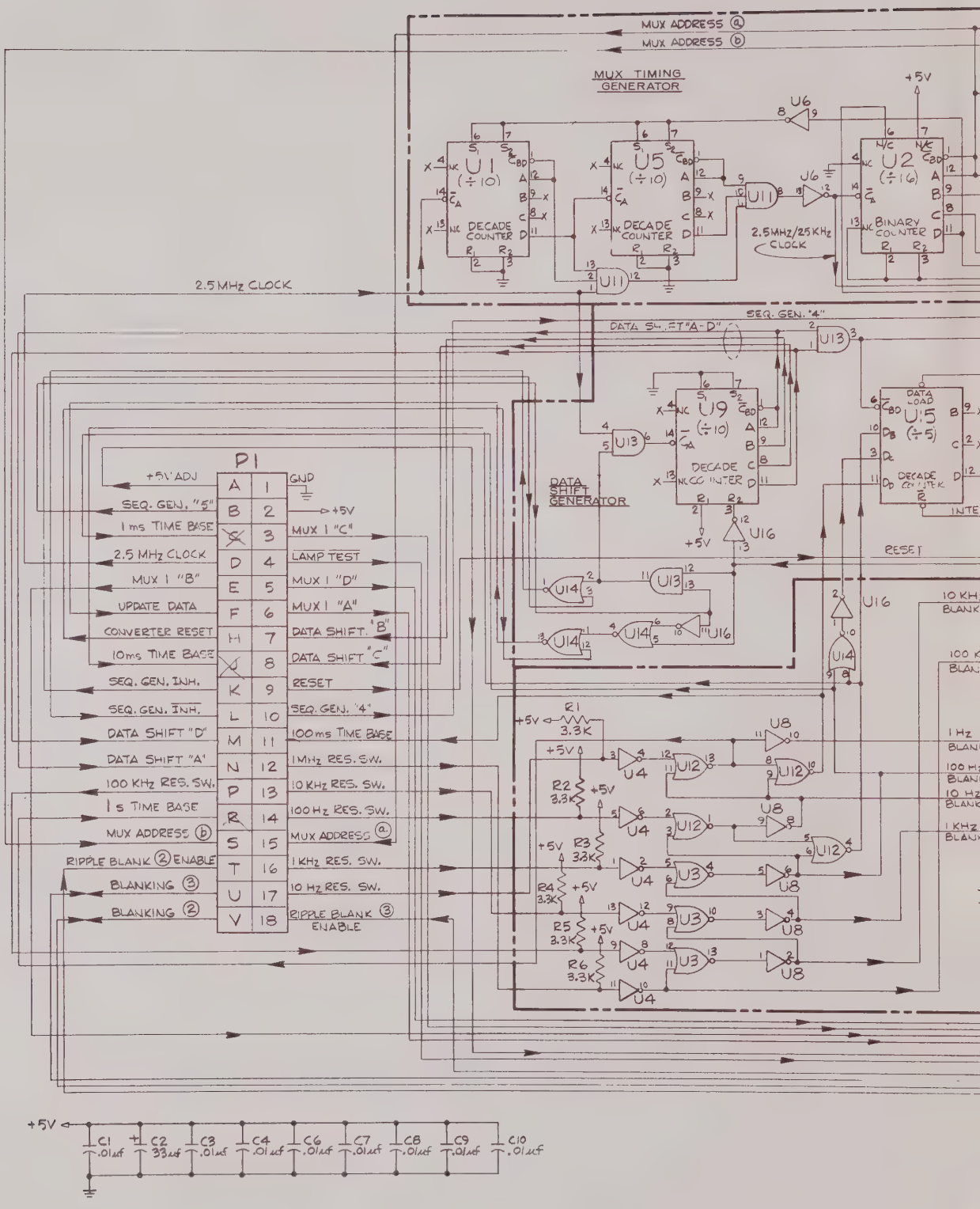


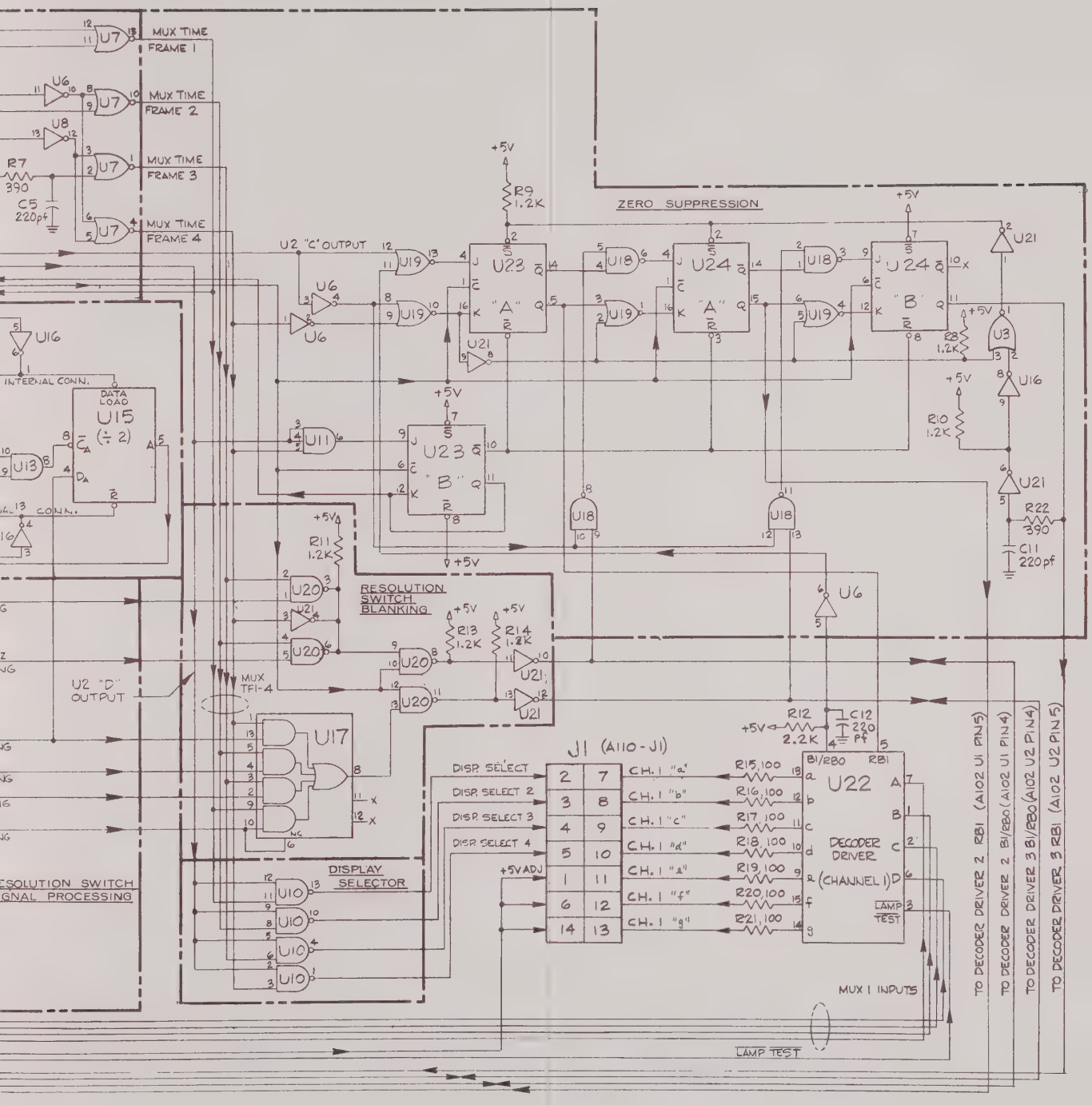
Figure 101a. Leading Zero Suppression Diagram



2020036 L

Figure 101b. Component Locator


MUX ADDRESS (a)
MUX ADDRESS (b)
MUX TIMING GENERATOR
+5V
U6
U1 (÷10) DECADE COUNTER
U5 (÷10) DECADE COUNTER
U11
U2 (÷16) BINARY COUNTER
2.5MHz/25KHz CLOCK
2.5 MHz CLOCK
SEQ. GEN. "4"
DATA SHIFT "A-D"
U13
U9 (÷10) DECADE COUNTER
DATA SHIFT GENERATOR
DATA LOAD
U15 (÷5) DECADE COUNTER
U16
RESET
U14
P1
+5V ADJ
GND
SEQ. GEN. "5"
+5V
1 ms TIME BASE
MUX 1 "C"
2.5 MHz CLOCK
LAMP TEST
MUX 1 "B"
MUX 1 "D"
UPDATE DATA
MUX 1 "A"
CONVERTER RESET
DATA SHIFT "B"
10ms TIME BASE
DATA SHIFT "C"
SEQ. GEN. INH.
RESET
SEQ. GEN. INH.
SEQ. GEN. "4"
DATA SHIFT "D"
100ms TIME BASE
DATA SHIFT "A"
1MHz RES. SW.
100 KHz RES. SW.
10 KHz RES. SW.
1 s TIME BASE
100 Hz RES. SW.
MUX ADDRESS (b)
MUX ADDRESS (a)
RIPPLE BLANK (2) ENABLE
1 KHz RES. SW.
BLANKING (3)
10 Hz RES. SW.
BLANKING (2)
RIPPLE BLANK (3) ENABLE
R1 3.3K
R2 3.3K
R3 3.3K
R4 3.3K
R5 3.3K
R6 3.3K
U4
U12
U3
U8
1 Hz BLANK
100 Hz BLANK
10 Hz BLANK
1 KHz BLANK
+5V
C1 .01uf
C2 33uf
C3 .01uf
C4 .01uf
C6 .01uf
C7 .01uf
C8 .01uf
C9 .01uf
C10 .01uf



5500036 D

Figure 101c. Schematic Diagram

A102
COUNT CHAIN 2

A102 is similar to A103, being simply a continuation of the counting chain that begins on A103. Six DCUs on A102 (U4, U7, U10, U12, U15, and U18) combine with the DCUs on A103 and A106 for a total of eight in the counter. Each of these six are presettable. They are programmed by data lines either from the Converter (when it is being used), or from external inputs when IF Offset Option 36 is used.

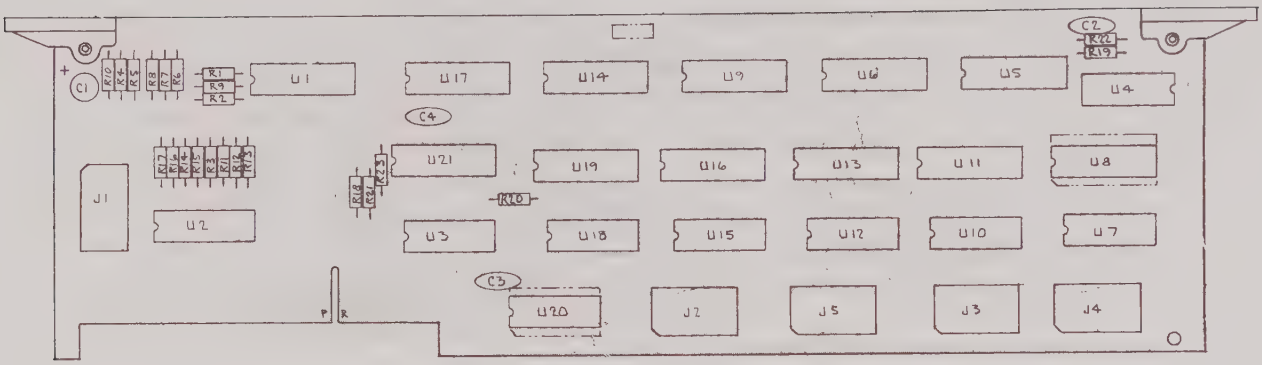
Each of the six DCUs has an associated quad-latch (U5, U8, U11, U13, U16, and U19) to store the DCU information. An additional latch (U21) stores the information from the DCU on A103 (U1). Two sets of multiplexers (U6 and U9, and U14 and U17) transfer the information from the latches to the display drivers. Two decoder-drivers (U1 and U2) convert the four line BCD information from the two multiplexers into the seven-line code necessary to drive the segments of the front panel display. Separate inputs to these decoders allow the display to be blanked, or to display all eights in the Visual Display Test. (A more detailed description will be found in the paragraphs titled "Leading Zero Suppression Circuitry" on the A101 theory of operation.

A102 Count Chain 2

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A102	Count Chain 2	2020034	1		
C1	Tant, 33μF, 10V	2300015	1	TAG 20-33/10-50	14433
C2 thru C4	Cer, .01μF, 20%, 100V	2150003	3	TG-S10	56289
J1 thru J5	14 Pin, Nylon	2630009	5	14-N-D1P	0000A
R1	Comp, 2.2K ohms, 5%	4010222	2	RC 07GF222J	81349
R2	Comp, 120 ohms, 5%	4010122	6	RC07GF121J	81349
R3	R1				
R4 thru R17	Comp, 100 ohms, 5%	4010101	1	RC07GF101J	81349
R18	R2				
R19	R2				
R20	Comp, 5.6 ohms, 5%	4010596	1	RC07GF5R6J	81349
R21	R2				
R22	R2				
R23	R2				
U1	BCD, 7 seg Decoder	3087447	2	DM74LS47	0000X
U2	U1				
U3	Hex Inverter	3087405	1	DM74LS05	0000X
U4	Preset DEC Counter	3074176	6	DM74176N	0000X
U5	Quad Latch	3087475	7	DM74LS75	0000X
U6	Dual 4/1 Multiplexer	3084153	4	DM74LS153	0000X
U7	U4				
U8	U5				
U9	U6				
U10	U4				
U11	U5				
U12	U4				
U13	U5				
U14	U6				
U15	U4				
U16	U5				
U17	U6				
U18	U4				
U19	U5				

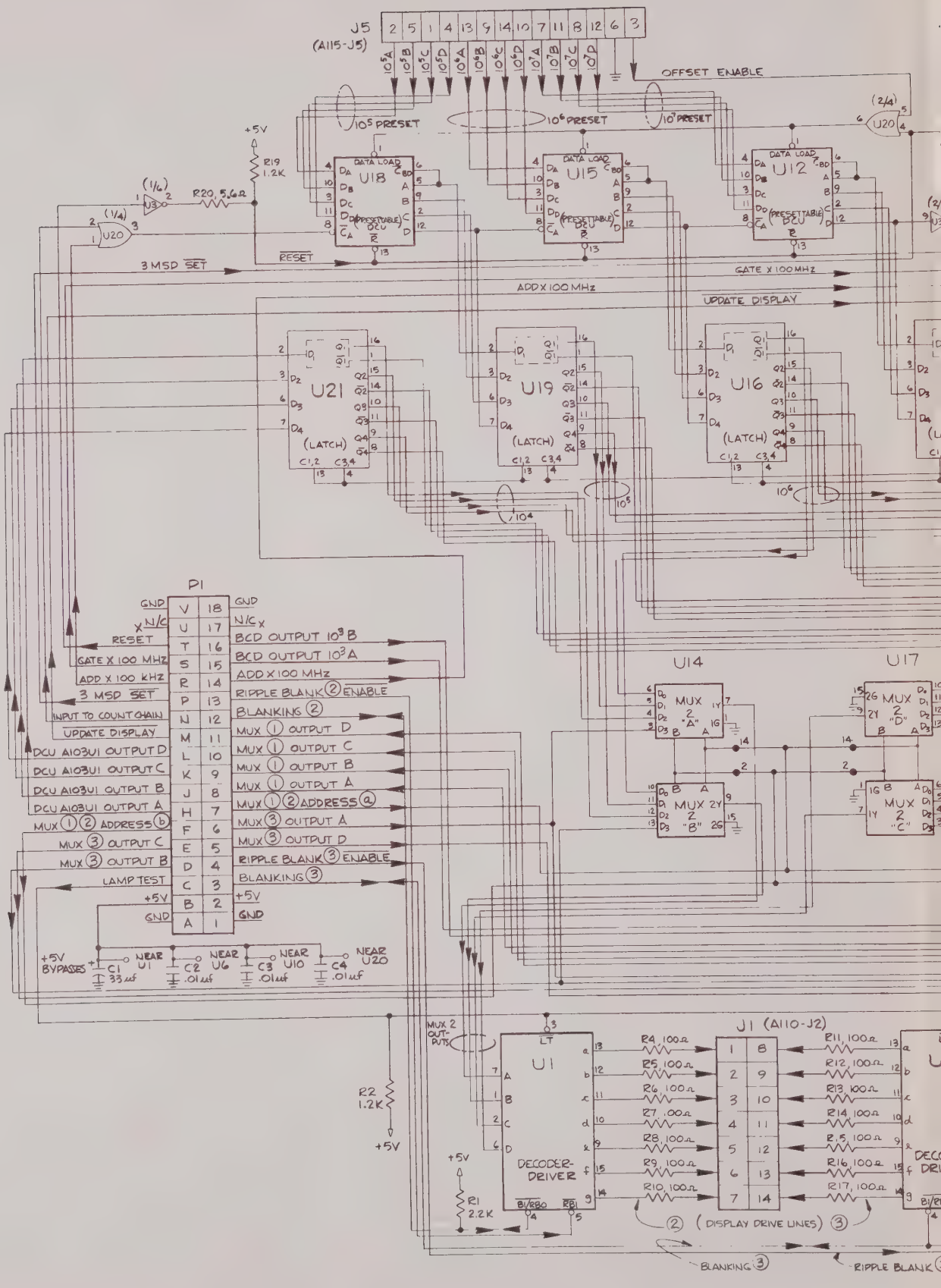
A102 Count Chain 2 (Continued)

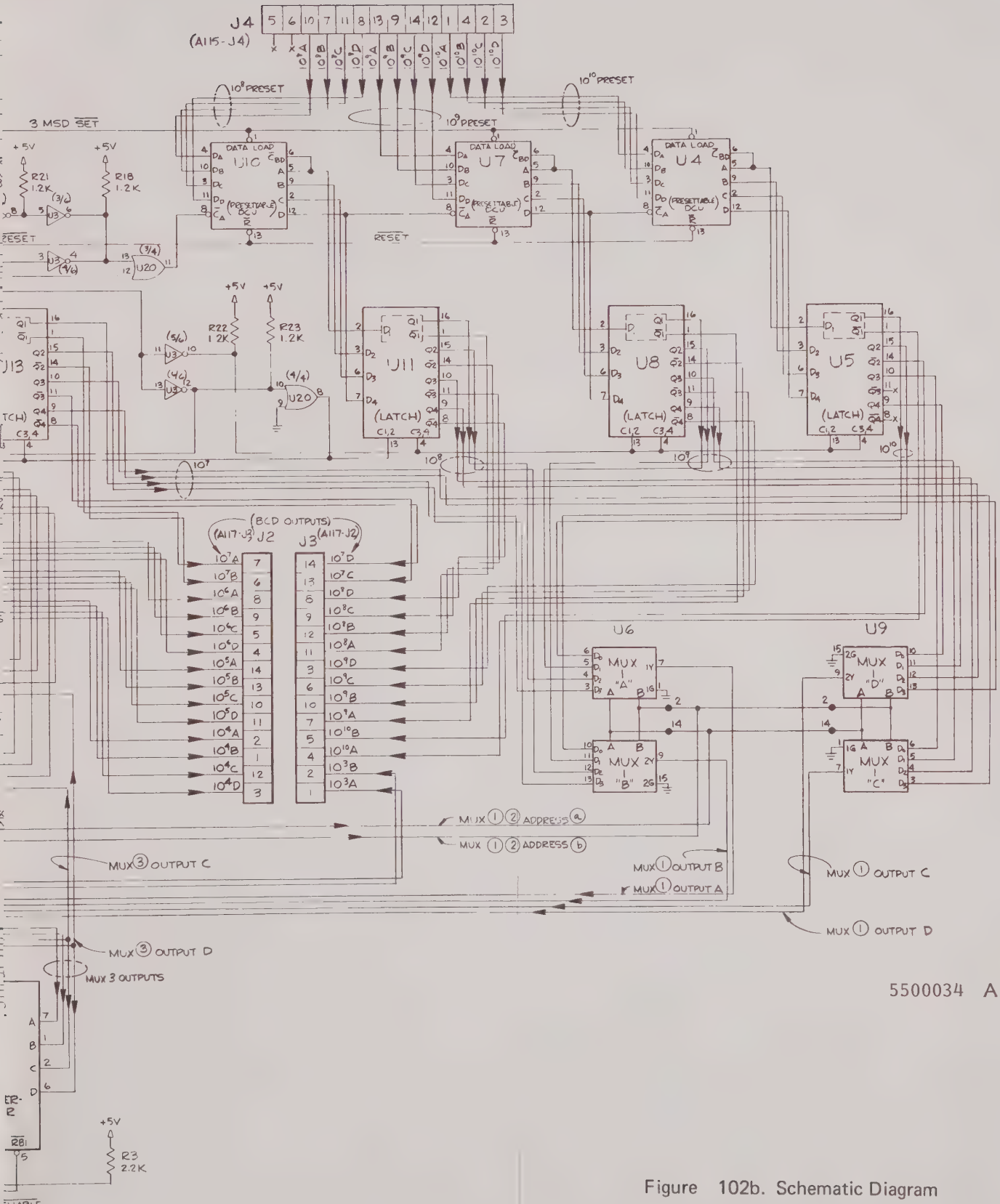
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U20 U21	Quad, 2INP OR Gate U5	3007432	1	DM7432N	0000X
	MISC				
	• Printed Circuit Board	5260034B			
	• Schematic	550034A			



2020034 F

Figure 102a. Component Locator


J5
(A115-J5)
OFFSET ENABLE
10⁵ PRESET
10⁶ PRESET
10⁷ PRESET
U18
U15
U12
U20
R19 1.2K
R20, 5.6Ω
3 MSD SET
RESET
GATE X 100 MHz
ADD X 100 MHz
UPDATE DISPLAY
U21
U19
U16
(LATCH)
P1
GND
N/C
RESET
GATE X 100 MHz
ADD X 100 kHz
3 MSD SET
INPUT TO COUNT CHAIN
UPDATE DISPLAY
DCU A103U1 OUTPUT D
DCU A103U1 OUTPUT C
DCU A103U1 OUTPUT B
DCU A103U1 OUTPUT A
MUX ① ② ADDRESS ⓑ
MUX ③ OUTPUT C
MUX ③ OUTPUT B
LAMP TEST
+5V
GND
BCD OUTPUT 10³ B
BCD OUTPUT 10³ A
ADD X 100 MHz
RIPPLE BLANK ② ENABLE
BLANKING ②
MUX ① OUTPUT D
MUX ① OUTPUT C
MUX ① OUTPUT B
MUX ① OUTPUT A
MUX ① ② ADDRESS ⓐ
MUX ③ OUTPUT A
MUX ③ OUTPUT D
RIPPLE BLANK ③ ENABLE
BLANKING ③
+5V BYPASSES
C1 33 µf
C2 .01 µf
C3 .01 µf
C4 .01 µf
NEAR U1
NEAR U6
NEAR U10
NEAR U20
U14
U17
MUX 2 "A"
MUX 2 "B"
MUX 2 "C"
MUX 2 "D"
MUX 2 OUTPUTS
U1
DECODER-DRIVER
R2 1.2K
R1 2.2K
J1 (A110-J2)
R4, 100Ω
R5, 100Ω
R6, 100Ω
R7, 100Ω
R8, 100Ω
R9, 100Ω
R10, 100Ω
R11, 100Ω
R12, 100Ω
R13, 100Ω
R14, 100Ω
R15, 100Ω
R16, 100Ω
R17, 100Ω
② (DISPLAY DRIVE LINES) ③
BLANKING ③
RIPPLE BLANK



5500034 A

Figure 102b. Schematic Diagram

A103
COUNT CHAIN 3

Count Chain 3 contains the second DCU in the count chain, the first latch for the storage circuit, the multiplexer for the least significant digit, and a variable power supply to adjust LED intensity.

The DCU carry signal from the high frequency board is translated from an ECL to a TTL level by transistors (Q1, Q2, and Q3). This signal enters DCU (U2). The outputs of U2 go to the A102 board to drive the rest of the count chain and the latch.

The 4 bit BCD output from the high frequency board drives a latch (U10). U13 and U14 convert the output of the latch to the proper multiplexed signal to drive the display.

Transistors (Q7 and Q8) form a supply variable from 0 to +5V which drives the anodes of the display LED's.

A103 Count Chain 3

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A103	Count Chain 3	2020051	1		
C1	Not Used				
C2	Not Used				
C3	Cer, .01μF, 20%, 100V	2150003	5	TG-S10	56289
C4	Tant, 33μF, 10%, 20V	2300015	2	TAG 20-33/10	56289
C5	C3				
C6	C3				
C7	Tant, 10μF, 25V	2300029	1	TAG 20-10/25M	14433
C8	C3				
C9	C4				
C10	C3				
CR1 thru CR8	Not Used				
CR9	General Purpose	2704154	1	1N4154	07264
J1	Socket, 14 pin 1C	2630009	2	14-N-DIP	71785
J2	J1				
Q1 thru Q3	Graded, 2N5179, Yellow	4710012	3	4705179	EIP
Q4	Not Used				
Q5	PNP, General Purpose	4704126	1	2N4126	04713
Q6	Not Used				
Q7	Q5				
Q8	NPN, Power	4710003	1	MJE 520	04713
R1	Comp, 130 ohms, 5%	4010131	1	RC07GF131J	81349
R2	Comp, 360 ohms, 5%	4010361	1	RC07GF361J	81349
R3	Comp, 20 ohms, 5%	4010200	1	RC07GF200J	81349
R4	Met. Ox., 220 ohms, 2%	4010221	1	C4/2%/220	81349
R5	Met. Ox., 120 ohms, 2%	4010121	1	C4/2%/120	81349
R6	Met. Ox., 430 ohms, 2%	4130431	1	C4/2%/430	24546
R7	Met. Ox., 470 ohms, 2%	4130471	1	C4/2%/470	24546
R8	Not Used				
R9	Comp, 2.2K ohms, 5%	4010222	2	RC07GF222J	81349
R10 thru R12	Not Used				
R13	R9				

Table of Contents, continued

Page

Appendix A – List of Manufacturers A-1

Appendix B – Options B-1

Option No.

13 Rack Mount/Chassis Slides B13-1
15 Automatic Input Level Control B15-1
16* General Purpose Interface Buss
31 Programming B31-1
32 YIG Preset – Thumbwheel B32-1
36 Programmable Offsets B36-1
39 BCD Output B39-1
40 Rear Panel Inputs B40-1

* See Separate Option 16 Manual.

List of Illustrations

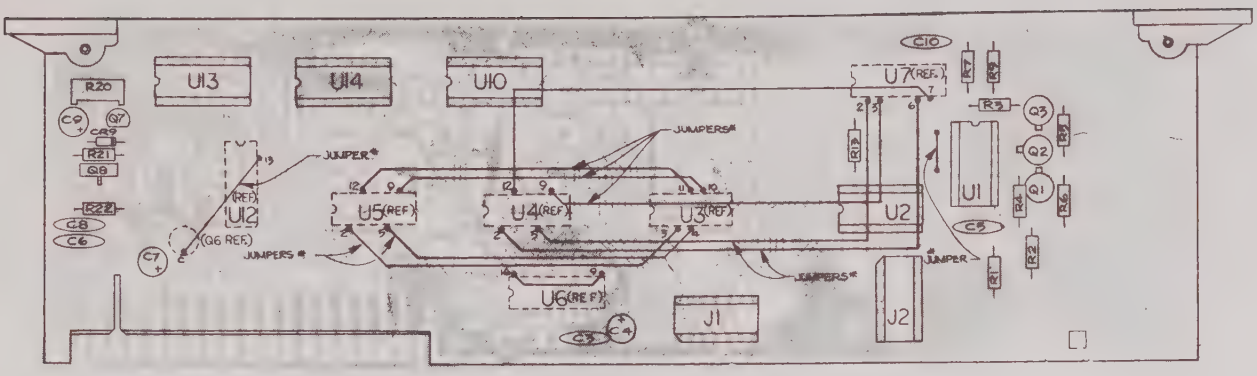
Figure No.		Page
3-1.	Front Panel	3-1
3-2.	Rear Panel	3-2
4-1.	Counter Block Diagram	4-1
4-2.	Autohet Converter Block Diagram	4-2
4-3.	YIG Filters	4-5
5-1.	Summing Amplifier	5-3
5-2.	Visual Display Test	5-7
5-3.	Missing Digit Test	5-8
5-4.	Non-Zero Display Test	5-10
5-5.	Self Test	5-11
5-6.	Converter Troubleshooting	5-12
6-1.	Calibration Adjustment Locator	6-1
6-2.	In-Band Detector Switching Point	6-3
6-3.	Typical Comb Level Adjustment	6-4
6-4.	1 GHz Comb Line Identification	6-5
6-5.	YIG Driver Offset Adjustment	6-6
6-6.	YIG Delay Correction 1	6-7
6-7.	YIG Delay Correction 2	6-7
6-8.	Comb Frequency Harmonic Generation	6-9
7-1.	331 Counter Interconnection Diagram	7-6

List of Tables

Table		Page
5-1.	Recommended Test Equipment	5-3
6-1.	Comb Level Adjustments	6-10

A103 Count Chain 3 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R14 thru R19	Not Used				
R20	Var Cer, 500 ohms	4250009	1	72XWR500	73138
R21	Comp, 820 ohms, 5%	4010821	1	RC07GF821J	81349
R22	Comp, 1K ohms, 5%	4010102	1	RC07GF102J	81349
R23	Not Used				
U1	Hex Inverter	3087405	1	DM74LS05	0000X
U2	PST, Decade Counter	3074196	1	DM74196N	0000X
U3 thru U9	Not Used				
U10	Quad Latch	3087475	1	SN74LS75	0000X
U11	Not Used				
U12	Not Used				
U13	Dual Multiplexer	3084153	2	DM74LS153	0000X
U14	U13				

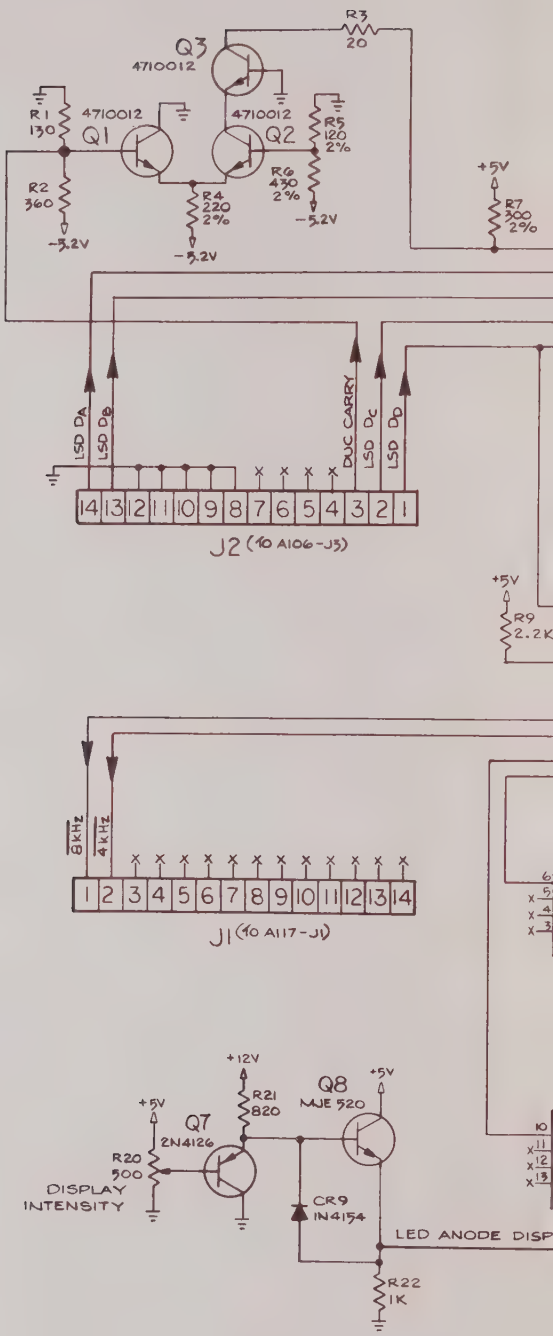


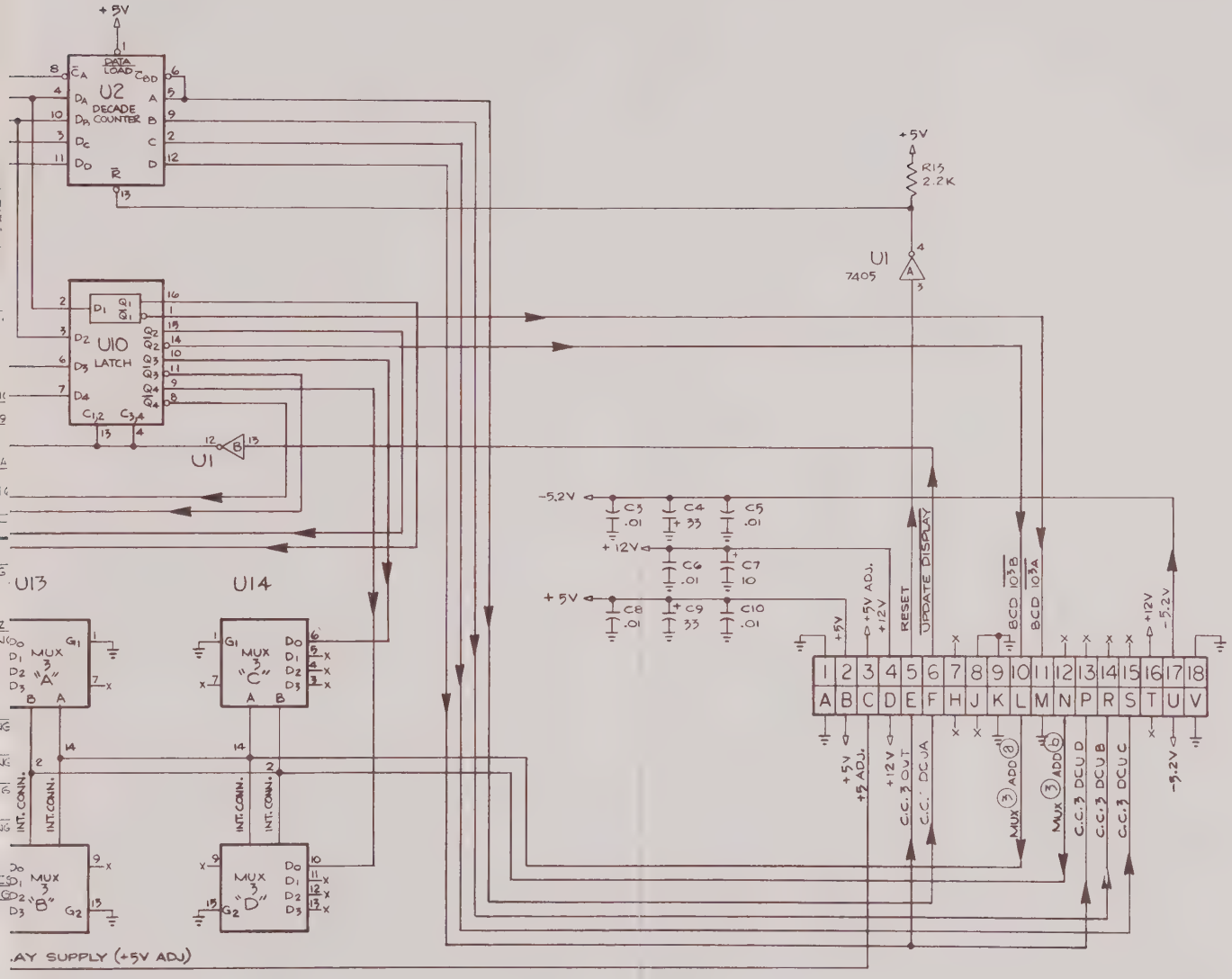
2020051-31 E

Figure 103a. Component Locator

SELECTED INPUT	ADDRESS	
	A	B
0	0	0
1	1	0
2	0	1
3	1	1

Table 103. Multiplex Address


R3
20
Q3
4710012
R1
130
4710012
Q1
4710012
Q2
R5
120
2%
R2
360
R4
220
2%
R6
430
2%
-5.2V
-5.2V
-5.2V
+5V
R7
300
2%
LSD DA
LSD DB
DUC CARRY
LSD DC
LSD DD
14 13 12 11 10 9 8 7 6 5 4 3 2 1
J2 (TO A106-J3)
+5V
R9
2.2K
8kHz
4kHz
1 2 3 4 5 6 7 8 9 10 11 12 13 14
J1 (TO A117-J1)
+12V
+5V
R21
820
Q8
MJE 520
+5V
Q7
2N4126
R20
500
DISPLAY
INTENSITY
CR9
IN4154
LED ANODE DISP
R22
1K



5500051-31 E

Figure 103b. Schematic Diagram

A104
CONTROL 2

This unit accepts front panel reset and test commands, programming inputs and internal control inputs. Internal control inputs to this unit are: SEQUENCE GENERATOR "0," SEQUENCE GENERATOR "5," SEQUENCE GENERATOR "8," PRINT command, and Converter LOCK. The outputs of A104 consist of counter control signals and a front panel SEARCH indicator.

CIRCUIT DESCRIPTION

The three Band Select input lines from P1 pins 6, 7 and 8, each drive an inverter in U1 when one particular line is grounded. The outputs drive the emitters of transistor switches Q1, Q2, and Q3. Their collectors connect directly to the Band Selection inputs on the High Frequency Board, and energize the appropriate input channel amplifier for that band. In the 331 counters the Band III , or converter input is always selected, disabling the other two inputs. The Q3 drive signal is combined with two other inputs via three inverters with open-collector outputs. The three inputs are the BAND III SELECT (always low), the LOCK signal (low when Converter is locked), and the TEST signal (low except in the TEST mode). The Converter must then be locked, and the unit *not* in the TEST mode, for the input to be enabled.

Manual Reset and Test inputs come from front panel RESET and TEST switches, and are fed through resistor-capacitor networks to Schmitt triggers composed of Q15, Q16, Q17, and Q8, Q9, Q10 respectively. These circuits are used to eliminate the effects of switch contact bounce.

The output of the TEST trigger generates the TEST command for A105, and the TEST signal. These signals are differentiated and fed to the base of Q11, which then triggers the RESET command at both start and finish of the TEST cycle. The TEST signal also drives the bases of Q1-Q3, disabling the input channels of A106 during the TEST cycle. Finally it combines with the Manual Reset to produce the Visual Display Test function of U7 pin 11.

The Manual Reset also drives the RESET trigger through C11 and Q12. This trigger drives the one shot U8 to produce the RESET pulse.

The CONVERTER RECYCLE command is generated at U7 pin 3, and is generated by either a Manual Reset, or after initial instrument turn on. At turn on, the circuit composed of Q4, Q5, and Q6 holds U8 in the triggered state for several seconds. This output sets the Sequence Generator on A105 to "9" and is equivalent to resetting the counter.

In Band III, a LOCK command is received from the Converter when a signal is acquired. This signal generates a RESET through Q14. It is also combined with the Band III SELECT command to drive the SEARCH indicator (U4 pin 8) on the front panel. In the event that the Converter loses LOCK, the one shot U6 is triggered. The output of U6 inhibits the Sequence Generator to allow the Converter to reacquire the signal without displaying zeros on the readout. If a LOCK command is not obtained within the one shot period, a RESET is generated via Q13. If a LOCK signal is reacquired, the delay time is reduced to a few milliseconds by Q18 and Q19.

In the event that the Sequence Generator is in the PRINT or memory update portion of the cycle when LOCK is lost, the sequence is allowed to continue to the Display period where it is held. This is accomplished by combining the PRINT command and SEQUENCE GENERATOR "5" in an OR gate, and then combining these with the output of U6 at U5 pin 11. When LOCK is reacquired, the counter is immediately reset.

A104 Control 2

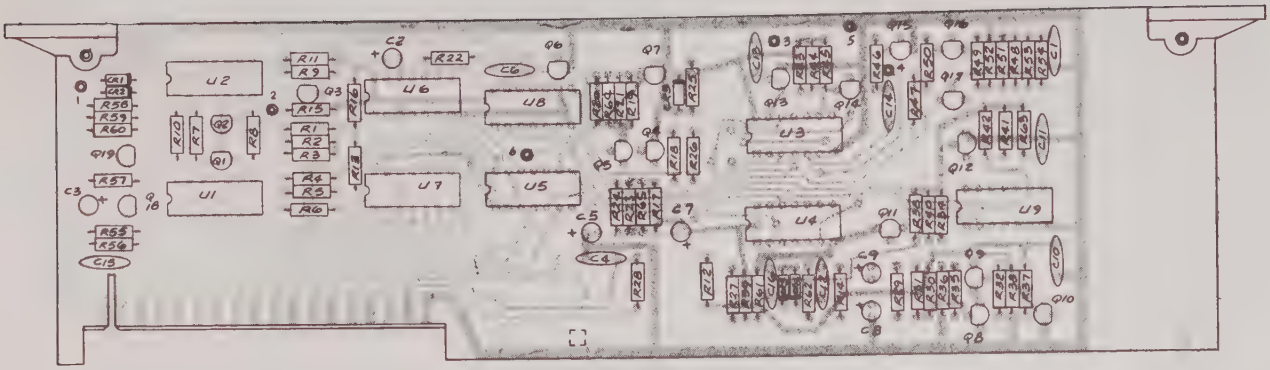
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A104	Control 2	2020010	1		
C1	Cer, .01μF, 20%, 100V	2150003	5	TG-S10	56289
C2	Tant, 33μF, 10V	2300015	2	TAG 20-33/10-50	14433
C3	C2				
C4	C1				
C5	Tant, 10μF, 25V	2300029	3	TAG 20-10/25	14433
C6	Cer, .001μF, 20%, 1KV	2150001	5	5GA-D10	56289
C7	Tant, 47μF, 6.3V	2300017	1	TAG 20-47/6.3-50	14433
C8	C5				
C9	C5				
C10	C1				
C11	C1				
C12 thru C14	C6				
C15	C1				
C16	C6				
CR1 thru CR5	GP	2704154	1	1N4154	07263
Q1 thru Q3	PNP GP	4704126	9	2N4126	04713
Q4	NPN GP	4704124	10	2N4124	04713
Q5	Q1				
Q6	Q4				
Q7	Q4				
Q8	Q1				
Q9	Q1				
Q10 thru Q15	Q4				
Q16 thru Q18	Q1				
Q19	Q4				
R1 thru R3	Comp, 2.2K ohms, 5%	4010222	15	RC07GF222J	81349

A104 Control 2 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R4 thru R6	Comp, 150 ohms, 5%	4010151	4	RC07GF151J	81349
R7 thru R9	Comp, 1K ohms, 5%	4010102	13	RC07GF102J	81349
R10	R1				
R11	Comp, 680 ohms, 5%	4010681	3	RC07GF680J	81349
R12	R1				
R13	R7				
R14	R4				
R15	R1				
R16	Comp, 47K ohms, 5%	4010473	1	RC07GF473J	81349
R17	R1				
R18	Comp, 2.7K ohms, 5%	4010272	3	RC07GF272J	81349
R19	R1				
R20	R1				
R21	R18				
R22	Comp, 10K ohms, 5%	4010103	9	RC07GF103J	81349
R23	R18				
R24	Comp, 100K ohms, 5%	4010104	1	RC07GF104J	81349
R25	R1				
R26	R1				
R27	Comp, 100 ohms, 5%	4010101	2	RC07GF101J	81349
R28	Comp, 5.6K ohms, 5%	4010562	10	RC07GF562J	81349
R29	R27				
R30	R22				
R31	Comp, 560 ohms, 5%	4010561	2	RC07GF561J	81349
R32	R7				
R33	R7				
R34	R28				
R35	R7				
R36	R11				
R37	R1				
R38	R28				
R39	R22				
R40	R28				
R41	R22				
R42	R28				
R43	R28				
R44	R22				
R45	R28				
R46	R22				

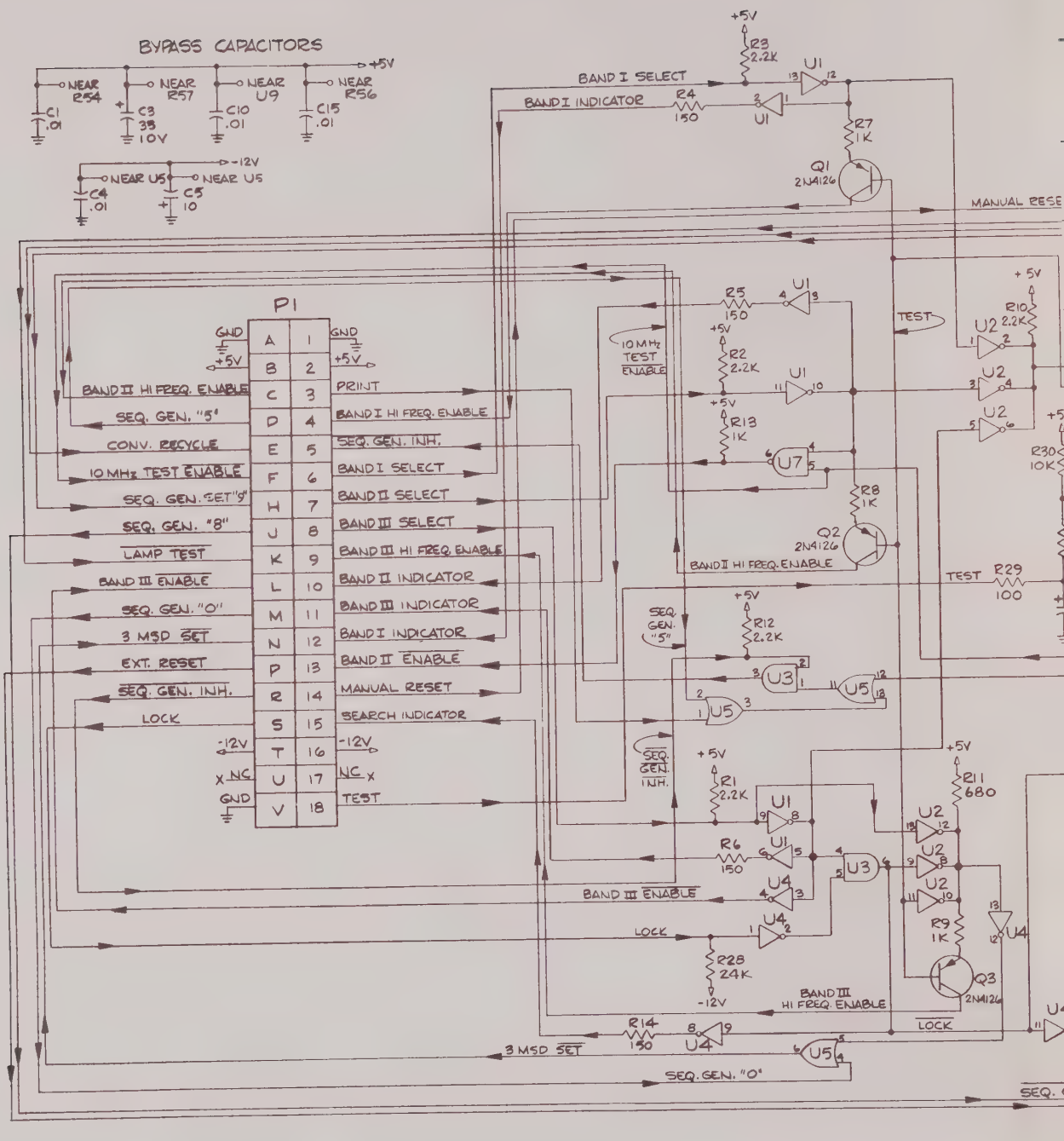
A104 Control 2 (Continued)

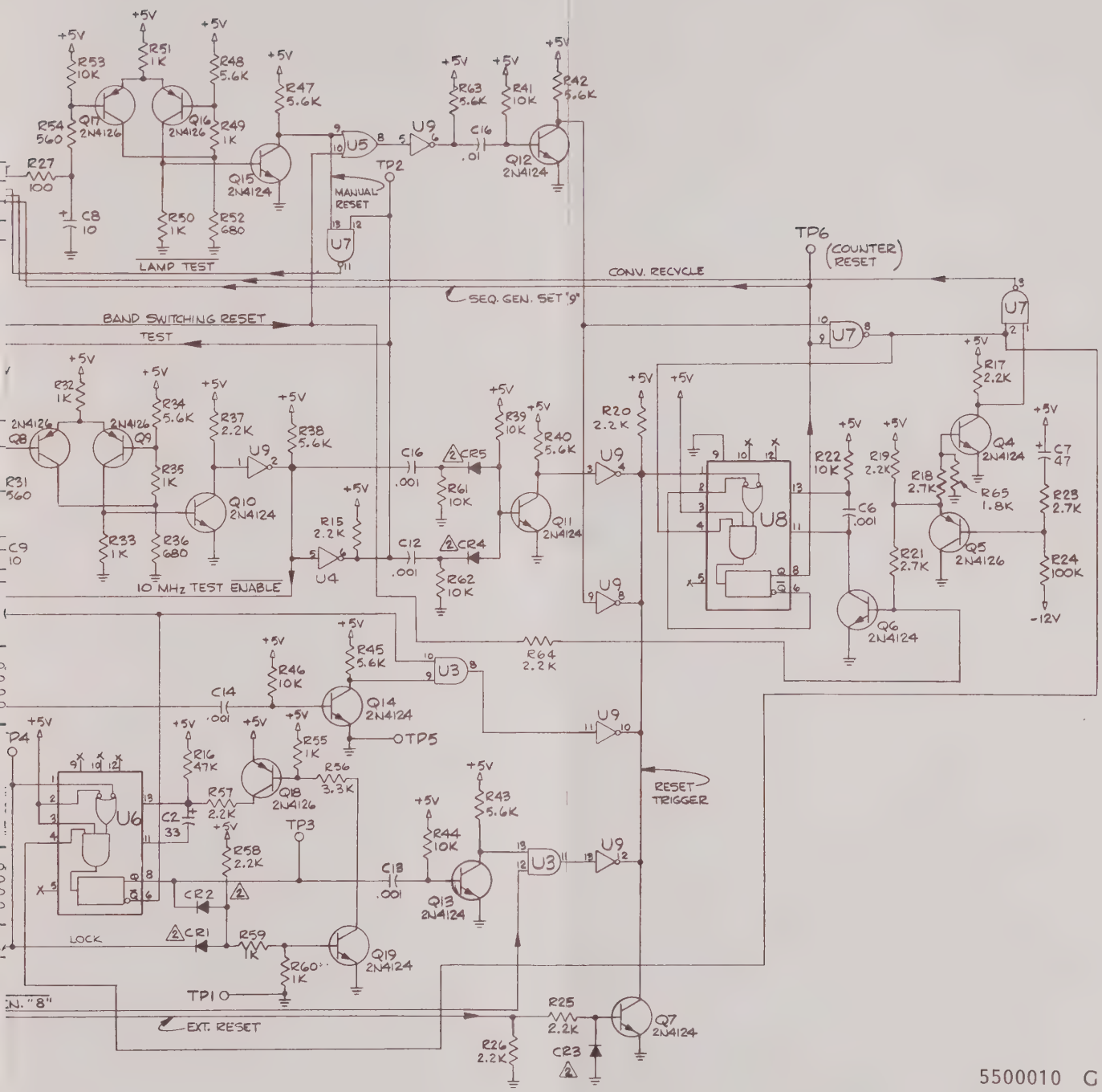
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R47	R28				
R48	R28				
R49	R7				
R50	R7				
R51	R7				
R52	R11				
R53	R22				
R54	R31				
R55	R7				
R56	Comp, 3.3K ohms, 5%	4010332	1	RC07GF332J	81349
R57	R1				
R58	R1				
R59	R7				
R60	R7				
R61	R22				
R62	R22				
R63	R28				
R64	R1				
R65	Comp, 1.8K ohms, 5%	4010182	1	RC07GF182J	81349
TP1 thru TP6	PC Pin, Gold	2620032	6	460-2970-0203	71274
U1	Hex Inverter	3087404	2	DM74LS04	0000X
U2	Hex Inverter	3087405	2	DM74LS05	0000X
U3	Quad, 21NP AND Gate	3087408	1	DM74LS08	0000X
U4	U1				
U5	Quad, 21NP OR Gate	3087432	1	DM74LS32	0000X
U6	Retrig One Shot	3008601	2	DM8601N	0000X
U7	Quad, 21NP NAND Gate	3087400	1	DM74LS00	0000X
U8	U6				
U9	U2				
	MISC				
	• Printed Circuit Board	5260010			
	• Schematic	5500010			



2020010 G

Figure 104a. Component Locator


BYPASS CAPACITORS
+5V
NEAR R54
NEAR R57
NEAR U9
NEAR R56
C1 .01
C3 33 10V
C10 .01
C15 .01
-12V
NEAR U5
NEAR U5
C4 .01
C5 10
P1
GND
+5V
BAND II HI FREQ. ENABLE
SEQ. GEN. "5"
CONV. RECYCLE
10 MHz TEST ENABLE
SEQ. GEN. SET "9"
SEQ. GEN. "8"
LAMP TEST
BAND III ENABLE
SEQ. GEN. "0"
3 MSD SET
EXT. RESET
SEQ. GEN. INH.
LOCK
-12V
X NC
GND
A 1
B 2
C 3
D 4
E 5
F 6
H 7
J 8
K 9
L 10
M 11
N 12
P 13
R 14
S 15
T 16
U 17
V 18
GND
+5V
PRINT
BAND I HI FREQ. ENABLE
SEQ. GEN. INH.
BAND I SELECT
BAND II SELECT
BAND III SELECT
BAND III HI FREQ. ENABLE
BAND II INDICATOR
BAND III INDICATOR
BAND I INDICATOR
BAND II ENABLE
MANUAL RESET
SEARCH INDICATOR
-12V
NC X
TEST
BAND I SELECT
BAND I INDICATOR
R3 2.2K
R4 150
R7 1K
Q1 2N4126
MANUAL RESE
R5 150
R2 2.2K
R13 1K
R8 1K
Q2 2N4126
BAND II HI FREQ. ENABLE
10 MHz TEST ENABLE
TEST
R10 2.2K
R30 10K
R29 100
R12 2.2K
SEQ. GEN. "5"
R1 2.2K
SEQ. GEN. INH.
R6 150
BAND III ENABLE
LOCK
R28 24K
-12V
R14 150
3 MSD SET
SEQ. GEN. "0"
R11 680
R9 1K
Q3 2N4126
BAND III HI FREQ. ENABLE
LOCK
SEQ.



5500010 G

Figure 104b. Schematic Diagram

A105
CONTROL 1

This unit contains the circuitry to generate the counter control sequence and the gate time interval. These functions are derived from the 10 MHz Time Base Oscillator.

CLOCK GENERATOR

Transistors Q1 through Q4 form a Schmitt Trigger to convert the 10 MHz time base signal to a square wave suitable to drive the ECL gates of U4. These outputs are further gated and translated to TTL levels in U8.

SEQUENCE GENERATOR

This circuit produces the main control cycle of the counter by generating a sequence of commands. It consists primarily of an address generator U9, and a decoder U12.

Clocking is performed at a 100 kHz rate by dividing the 10 MHz TTL clock in DCU's U2 and U7. An output of 2.5 MHz is also obtained at U7 pin 12 for the multiplexer clock on Count Chain 1 (A101). The gates of U5 are arranged so that both the 100 kHz and the 2.5 MHz signals are trains of 50 ns wide pulses.

The 100 kHz pulse train drives address generator U9, which produces a four line BCD code. The A and B outputs of U9 address U12, while the C output selects which of the two decoders is active. This generates sequential control signals, one on each of eight lines. Two more signals are obtained using the D output of U9 by itself, or combined with the A output. The gate inputs to U12 (pins 2 and 14) are turned off during switching and when not required, by an OR gate in U13. This eliminates any outputs due to switching transients.

Several internal counter operations inhibit the sequence generator. In addition, Digital Output Option 39 and Programming Option 31, allow the sequence to be externally inhibited.

GATE GENERATOR

The Gate Generator provides the correct gate time interval. The time interval is controlled by selecting an integral number of cycles of the 10 MHz Time Base Oscillator. This then turns the Gate Binary U10 on and off appropriately.

The major element of the Gate Generator is a programmable multi-decade divider, U19. By applying the proper address a division ratio of 10^3 can be obtained. A 1 MHz input is then used to generate intervals of 1 ms. DCU U16 divides the 10 MHz clock signal to provide the 1 MHz input for U19. The address is obtained by processing the four gate control signals from A101.

The Q_B output of U22 is combined in U17 with the 10 MHz clock and the A and D outputs of U16 to produce the Time Base Gate Level at U17 pin 6. This arrangement guarantees that the gate time interval is precisely determined by the 10 MHz signal itself.

It is necessary that the Q_B output be no more than one microsecond duration. The two flip-flops of U22 are interconnected in such a manner as to produce a single one microsecond pulse every time the output of U19 goes low.

DISPLAY TIME GENERATOR

This generator consists of U18, U15, Q6, Q7 and associated circuitry. Triggering the multivibrator U18 generates a pulse whose width is determined by C21 and the resistance of the front panel SAMPLE RATE potentiometer. Q6 is a current amplifier to increase the available range, while DCU U15 is used to scale the range by a factor of ten. The result is a display time period variable from approximately 60 ms to 40 seconds. U18 is triggered by the SEQUENCE GENERATOR "8" appearing at pin 2. Once turned on, feedback from Q7 to pin 4 holds the unit in its free running state until pin 3 goes low. Pin 3 input is derived from the output of DCU U15. The Display Time Generator output (U3 pin 12) is then used as one of the Sequence Generator Inhibit inputs.

The Display Time cycle begins with SEQUENCE GENERATOR "9" setting U15 (pin 7) to the "9" state which inhibits U18 (pin 3) from triggering. When SEQUENCE GENERATOR "7" begins, U15 is reset (pin 3), thus enabling U18. Period "8" triggers U18 (pin 2) and the Sequence Generator is then held in period "8" until U15 counts to 9, at which time the display period ends.

Application of the front panel HOLD command at U13 pin 8, holds U15 in the reset position so that the Sequence Generator is permanently inhibited in period 8.

Table 105a. Sequence Generator Commands

PERIOD	FUNCTION	DURATION	LOCATION
9	COUNTER RESET	10 μs	
0	3 MSD SET	10 μs	U12 pin 9
1	OFFSET ENABLE	10 μs	U12 pin 10
2	GATE GENERATOR $\overline{\text{SET}}$	10 μs	U12 pin 11
3	GATE GENERATOR ENABLE	10 μs	U12 pin 12
4	GATE PERIOD	GATE +10 μs	U12 pin 7
5	$\overline{\text{DATA UPDATE}}$	10 μs	U3 pin 10
6/7	PRINT	20 μs	U14 pin 6
8	DISPLAY PERIOD	Variable	U9 pin 11

Commands are generated as shown in Table 105-a. (Period numbering is determined by the output state of U9.) The sequence proceeds as follows:

Period 9: The starting point in the cycle. All counting chain DCU's are reset.

Period 0: The YIG/Comb Generator frequency is preset.

Period 1: Used to preset counter in conjunction with Offset Option 36.

Period 2: The Gate Generator is set.

Period 3: The Latch Binary (U10B) is reset, enabling the Gate Binary (U10A). The 10 MHz clock (U8 pin 7) is applied to the Gate Generator.

Period 4: The Gate Generator is enabled and inhibits the Sequence Generator (U13 pin 8) for the duration of the gate time. The incoming signal to the counter is counted during this period.

Period 5: The accumulated data is the counting chain DCU's is loaded into the latches.

Period 6/7: The PRINT command is generated indicating the presence of data on units equipped with Digital Output Option 39.

Period 8: The Display Period. The Display Generator is turned on and inhibits the Sequence Generator during this time. The duration of the period is determined by the front panel SAMPLE RATE control.

A105 Control 1

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A105	Control 1	2020009	1		
C1	Cer, .01μF, 20%, 100V	2150003	15	TG-S10	56289
C2	C1				
C3					
C4 thru C6	C1				
C7	Mica, 10pF, 5%, 500V	2250001	4	DM15CD100D0	72136
C8 thru C11	C1				
C12	C7				
C13	Tant, 33μF, 10V	2300015	2	TAG 20-33/10-50	14433
C14	C7				
C15	C1				
C16	C7				
C17	C1				
C18	C1				
C19	C3				
C20	C1				
C21	C3				
C22	C1				
C23	C13				
C24	C1				
C25	C3				
J1	14 pin, Nylon	2630009	1	14-N-DIP	0000A
Q1	PNP RF	4704258	2	2N4258	07263
Q2	MTCH PR, 2NS179 Red	4710014	2	2N5179	04713
Q3	Q1				
Q4	Q2				
Q5	PNP GP	4704126	1	2N4126	04713
Q6	NPN GP	4704124	2	2N4124	04713
Q7	Q6				
R1	Comp, 15K ohms, 5%	4010153	1	RC07GF153J	81349
R2	Comp, 220 ohms, 5%	4010221	1	RC07GF221J	81349
R3	Comp, 68 ohms, 5%	4010680	1	RC07GF680J	81349
R4	Comp, 560 ohms, 5%	4010561	2	RC07GF561J	81349
R5	Comp, 100 ohms, 5%	4010101	2	RC07GF101J	81349
R6	Comp, 270 ohms, 5%	4010271	1	RC07GF271J	81349

A105 Control 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R7	Comp, 330 ohms, 5%	4010331	3	RC07GF331J	81349
R8	Comp, 150 ohms, 5%	4010151	1	RC07GF151J	81349
R9 thru R11	Comp, 470 ohms, 5%	4010471	3	RC07GF471J	81349
R12	R7				
R13	R5				
R14	R7				
R15	Comp, 820 ohms, 5%	4010821	5	RC07GF182J	81349
R16	Comp,1.2K ohms, 5%	4010122	4	RC07GF122J	81349
R17	Comp, 1.8K ohms, 5%	4010182	1	RC07GF182J	81349
R18	Comp, 1K ohms, 5%	4010102	9	RC07GF102J	81349
R19	R18				
R20	Comp, 3.3K ohms, 5%	4010332	9	RC07GF332J	81349
R21	R15				
R22	R16				
R23	R20				
R24	Comp, 390 ohms, 5%	4010391	4	RC07GF391J	81349
R25	R24				
R26	Comp, 10K ohms, 5%	4010103	2	RC07GF103J	81349
R27	R4				
R28	R24				
R29	R20				
R30	R18				
R31	R18				
R32	Comp, 2.2K ohms, 5%	4010222	8	RC07GF222J	81349
R33	R20				
R34	R24				
R35	R15				
R36	R16				
R37	R18				
R38	R20				
R39	R18				
R40	R20				
R41	R18				
R42	R18				
R43	R20				
R44	R15				
R45	R16				
R46	R20				
R47 thru R49	R32				

A105 Control 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R50	R26				
R51	R32				
R52	R32				
R53	R15				
R54	R20				
R55	R18				
R56	R32				
R57	R32				
R58	Comp, 4.7K ohms, 5%	4010472	1	RC07GF472J	81349
R59	Comp, 1.6K ohms, 5%	4010162	1	RC07GF162J	81349
U1	One Shot, Retrig	3008601	2	DM8601N	0000X
U2	Decade Counter	3087490	5	DM74LS90	0000X
U3	Quad, NOR Gate	3087402	2	DM74LS02	0000X
U4	Tri, OR Gate	3110150	1	MC10105L	
U5	Quad, AND Gate	3090002	2	DM74H08N	0000X
U6	Hex Inverter	3087404	3	DM74LS04	0000X
U7	U2				
U8	Quad, Translator	3011039	1	MC1039P	0000X
U9	U2				
U10	Dual D F/F	3110131	1	MC10131L	0000X
U11	U6				
U12	Dual 2/4 Line Decoder	3084155	1	DM74LS155	0000X
U13	Quad, OR Gate	3087432	1	DM74LS32	0000X
U14	Quad, NAND Gate	3087400	1	DM74LS00	0000X
U15	U2				
U16	U2				
U17	U5				
U18	U1				
U19	P CHAN, MOS Divider	3035009	1	MK5009P	0000X
U20	U6				
U21	U3				
U22	Dual J-K F/F	3087476	1	DM74LS76	0000X
	MISC				
	• Printed Circuit Board	5260009	1		
	• Schematic	5500009	REF		

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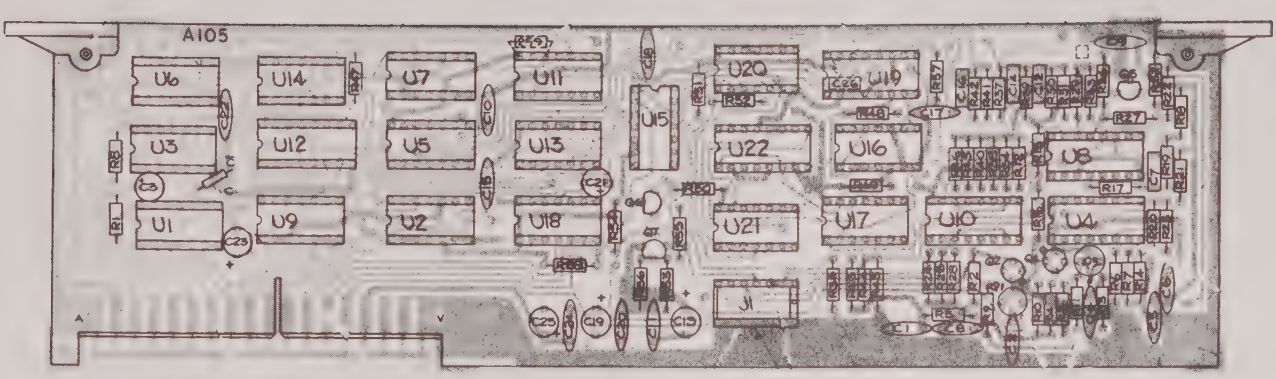
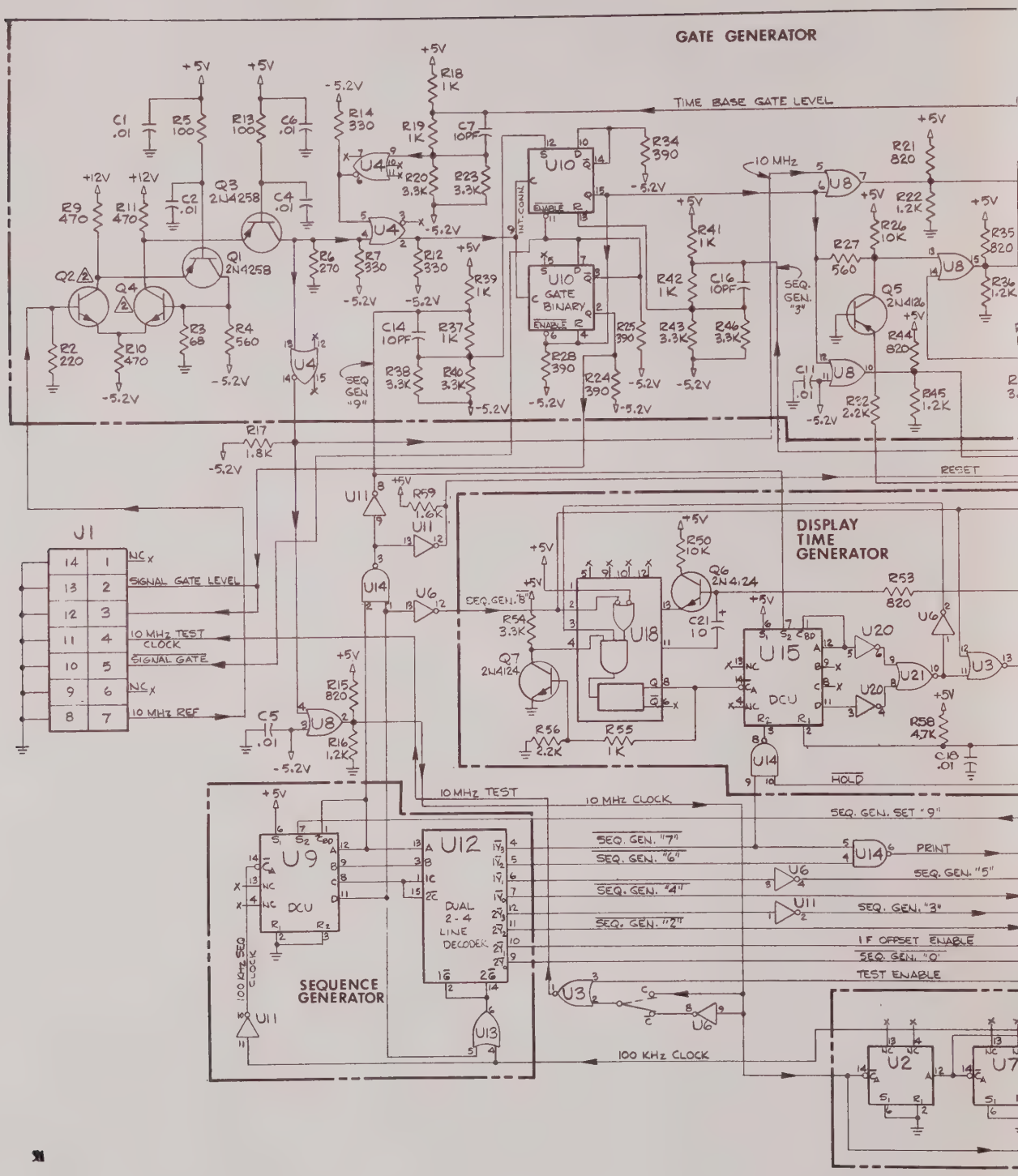


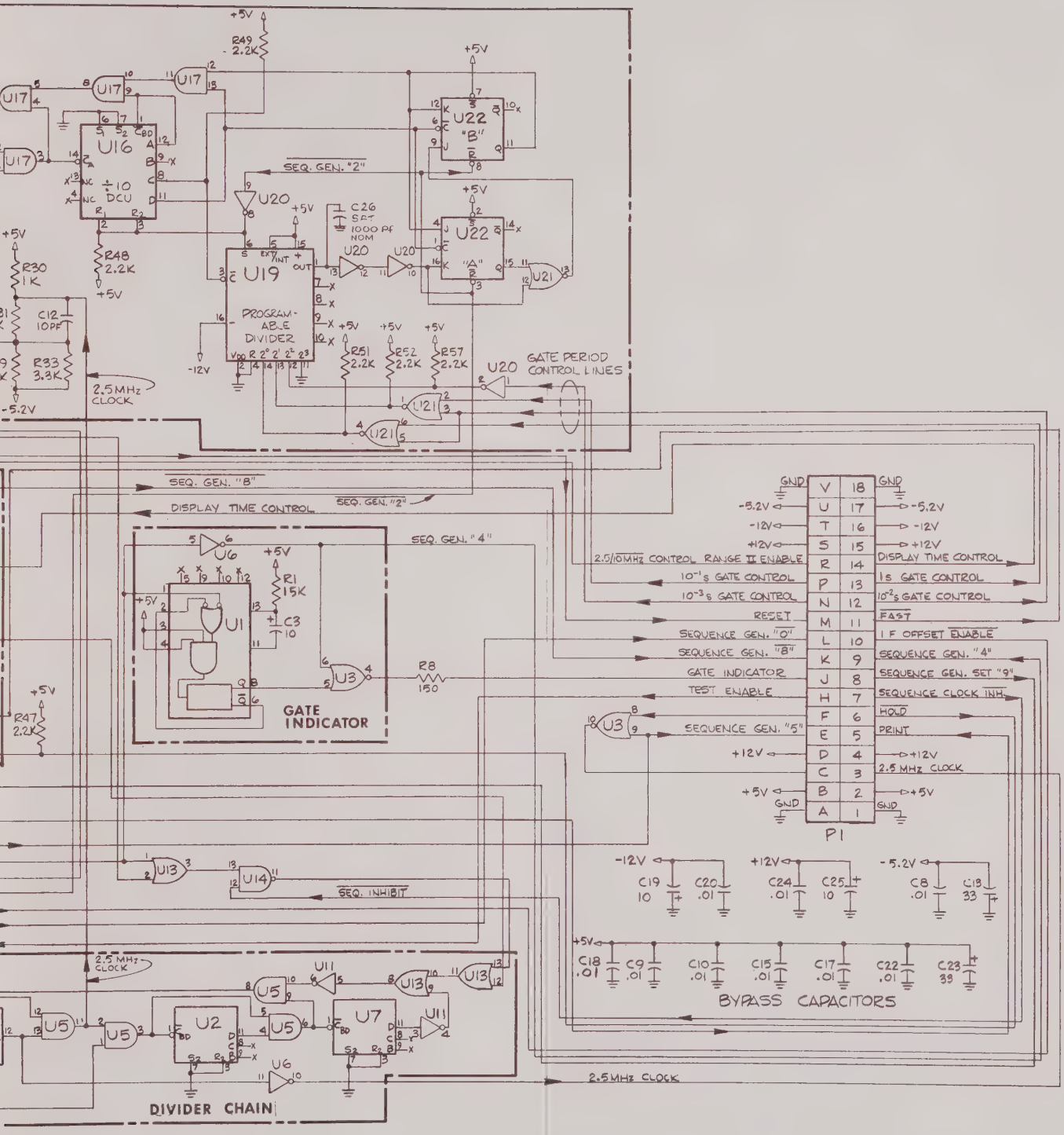
2020009 V

Figure 105a. Component Locator

CONTROL LINE			DIVISION RATIO
2^0	2^1	2^2	
1	1	0	10^3
0	0	1	10^4
1	0	1	10^5
0	1	1	10^6

Table 105b. Programmable Divider


GATE GENERATOR
TIME BASE GATE LEVEL
10 MHz
SEQ. GEN. "3"
SEQ. GEN. "9"
INT. CONN.
U10 GATE BINARY
ENABLE
RESET
DISPLAY TIME GENERATOR
SEQ. GEN. "8"
Q6 2N4124
Q7 2N4124
U18
U15 DCU
U20
U21
HOLD
J1
NC
SIGNAL GATE LEVEL
10 MHz TEST CLOCK
SIGNAL GATE
NC
10 MHz REF
10 MHz TEST
10 MHz CLOCK
SEQ. GEN. SET "9"
SEQ. GEN. "7"
SEQ. GEN. "6"
SEQ. GEN. "4"
SEQ. GEN. "2"
PRINT
SEQ. GEN. "5"
SEQ. GEN. "3"
IF OFFSET ENABLE
SEQ. GEN. "0"
TEST ENABLE
100 KHz CLOCK
SEQUENCE GENERATOR
U9 DCU
U12 DUAL 2-4 LINE DECODER
100 KHz SEQ CLOCK
U2
U7



5500009 N

Figure 105b. Schematic Diagram

A106
HIGH FREQUENCY

The High Frequency Board accepts RF signals from the Converter (A2), and gate and 10 MHz Test Signals from Control 1 (A105). Enable signals from Control 2 (A104) select the appropriate input which is processed, gated, and counted in the first decade counting unit (DCU). The outputs from A106 are the carry (f/10) signal, and the first decade of BCD information. These signals go to Count Chain 3 (A103) for further processing.

A106 accepts input signals on J4, and a 10 MHz Test signal on J3 pin 4. The input on U4 is selected by a command signal entering on pin 12 of P1. The command line sits at approximately -12V until it is selected, at which time it is pulled up to about +0.7V. This command signal, through the appropriate resistor divider, brings the base of a current source transistor up to about -6V, turns on the appropriate differential amplifier, and allows a signal to pass through. The signal entering the gated amplifier is terminated with a 51 ohm resistor, and a small inductor in series with the resistor to compensate for transistor loading at high frequencies. The net combination keeps the input VSWR below 1.5:1 up to 400 MHz. The input is deselected when 10 MHz test is enabled.

The input amplifier differentially drives squaring circuit Q3 and CR6. Q3 is a current mirror which is used as a voltage-to-current converter. The current from Q3's collector is used to drive tunnel diode CR6. The action of a tunnel diode under a current driving signal is that of a Schmitt trigger; that is, the voltage across the diode changes abruptly between two states ($<$0.2 and 1V). This characteristic converts the sine wave current into a square wave voltage signal, which can be used to drive the pulse forming network.

The pulse forming network input is a wide-band high speed differential amplifier (Q4/Q5), to increase the amplitude of the tunnel diode signal, and improve the rise and fall times. The output of Q4/Q5 drives current mirror Q6, used here as a current switch. Essentially, Q6 is either on or off, but the output is the current from the collector, and not a voltage signal. The switched current signal drives differentiator L7. The output of a differentiator with a square wave input is a series of pulses — positive when Q6 turns on, and negative when Q6 turns off. The negative pulses (wider than the positive pulses due to transistor storage time) are removed by CR9. Shorting out the negative pulses also provides a damping effect on L7, improving its response to the positive pulses at high frequencies.

These positive pulses are then coupled to pulse inverter Q7, which has two functions, to invert the pulse, and to deliver the negative output pulses at the right dc reference level for decade divider U3. A stable dc reference is provided by resistive divider R43, R44, and R45. The voltage from this divider is as stable over time and temperature as the -12V power supply. The inverter is kept from disturbing this reference by being biased just at cutoff. This

is accomplished by developing a forward bias for the transistor from the voltage drop across CR10, whose voltage matches the base-emitter voltage of Q7, keeping Q7 just at the edge of conduction. Basically, Q7 is a pulse amplifier, since it only conducts during a signal pulse. The load resistor for Q7 is the net equivalent of the bias network R43-R45.

Q7 output drives the input of decade divider U3. The divide-by-ten output of U3 is a 60/40% duty cycle ECL level signal, and is called the "DCU CARRY" signal (J3 pin 3); the load resistor for this signal is located on A103.

The gate signal to the DCU is an inverted ECL signal. It enters on J3 pin 5, and goes directly to U3 pin 16. The BCD output information is available at J3 pins 1, 2, 13, and 14. During a count cycle at high frequencies, this information is slew rate limited, and actual output level cannot be seen until the circuit comes to rest. After the circuit is finished counting, TTL level signals are present at these outputs. U3 is reset after the counting cycle is complete by a TTL reset signal at pin 3.

A106 High Frequency

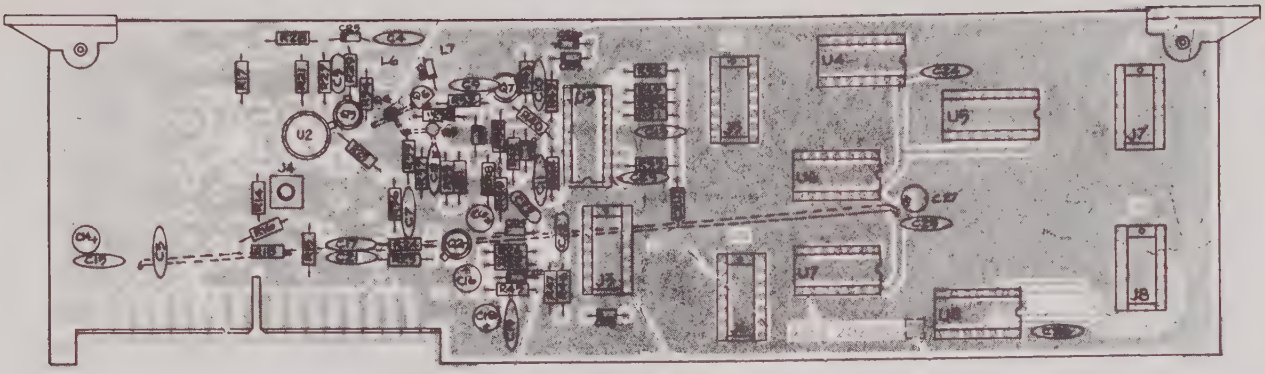
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A106	High Frequency	2020068	1	EIP	
C1	Not Used				
C2	Not Used				
C3	Cer, .01μF, 20%, 100V	2150003	11	TG-S10	56289
C4	C3				
C5	Mica, 10pF, 5%, 500V	2250001	1	DM15CD100DO	72136
C6	Tant, 10pF, 16V	2300010	3	TAG 20-10/16	14433
C7	C3				
C8	C3				
C9	Cer, .001μF, 20%, 1KV	2150001	2	5GA-D10	56289
C10	C3				
C11	C3				
C12	Mica, S.A.T.	2250999	1	DM15CDXXXCD	72136
C13	C3				
C14	C6				
C15	C3				
C16	C6				
C17	C3				
C18	Tant, 33μF, 10V	2300015	1	TAG 20-33/10	14433
C19	C3				
C20	Not Used				
C21	C3				
C22	Mica, 100pF, 5%, 500V	2250002	1	DM15CD101JO	72136
C23	C9 (for Op 16 only)		1		
C24 thru C26	C3 (for Op 16 only)		1 3		
C27	C18 (for Op 16 only)		1		
CR1 thru CR4	Not Used				
CR5	G.P.	2704151	7	1N4154	07263
CR6	Not Used				
CR7	CR5				
CR8	ZEN, 6.2V	2705234	1	1N5234	04713
CR9	Hot Carrier	2710016	2	5082-2835	28480
CR10	CR5				
CR11	ZEN, 4.7V	2705230	1	1N5230	04713
CR12	CR5				
CR13	CR9				

A106 High Frequency (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
CR14 thru CR16	CR5				
J3	Socket, 14 Pin	2630009	1	(Qty. 5 for Op 16)	71785
J4	Conn, PC JK RCPT	2610018	1	51-051-0000	98291
J5 thru J8	J3 (for Op 16 only)				
Q1	Not Used				
Q2	Graded, 2N5179-Red	4710011	1	4705179	EIP
Q3	PNP, RF	4704959	1	2N4959	04713
Q4	NPN, RF, SW	4710017	2	MMT 3960	04713
Q5	Q4				
Q6	PNP, RF	4710010	1	MPS-H81	04713
Q7	Graded, 2N5179-Green	4710013	1	4705179	EIP
R1 thru R13	Not Used				
R14	Comp, 51 ohms, 5%	4010510	1	RC07GF510J	81349
R15	Comp, 3K ohms, 5%	4010302	1	RC07GF302J	81349
R16	Comp, 2.7K ohms, 5%	4010272	2	RC07GF272J	81349
R17	Comp, 510 ohms, 5%	4010511	2	RC07GF511J	81349
R18	Comp, 5.6 ohms, 5%	4010596	5	RC07GF596J	81349
R19	Not Used				
R20	Not Used				
R21	R16				
R22	Comp, 470 ohms, 5%	4010471	1	RC07GF471J	81349
R23	Met Ox, 300 ohms, 2%	4130301	1	C4/2%/300	24546
R24	Met Ox, 2.7K ohms, 2%	4130272	1	C4/2%/2.7K	24546
R25	Met Ox, 820 ohms, 2%	4130821	1	C4/2%/820	24546
R26	Comp, 100 ohms, 5%	4010101	2	RC07GF101J	81349
R27	Met Ox, 68 ohms, 2%	4130680	1	C4/2%/68	24546
R28	R18				
R29	Met Ox, 43 ohms, 2%	4130430	1	C4/2%/43	24546
R30	Met Ox, 56 ohms, 2%	4130560	2	C4/2%/56	24546
R31	R18				
R32	R30				
R33	Met Ox, S.A.T., 5%	4130999	1	C4/2%/(1.1K Nom.)	24546
R34	R26				
R35	Comp, 430 ohms, 5%	4010431	2	RC07GF431J	81349

A106 High Frequency (Continued)

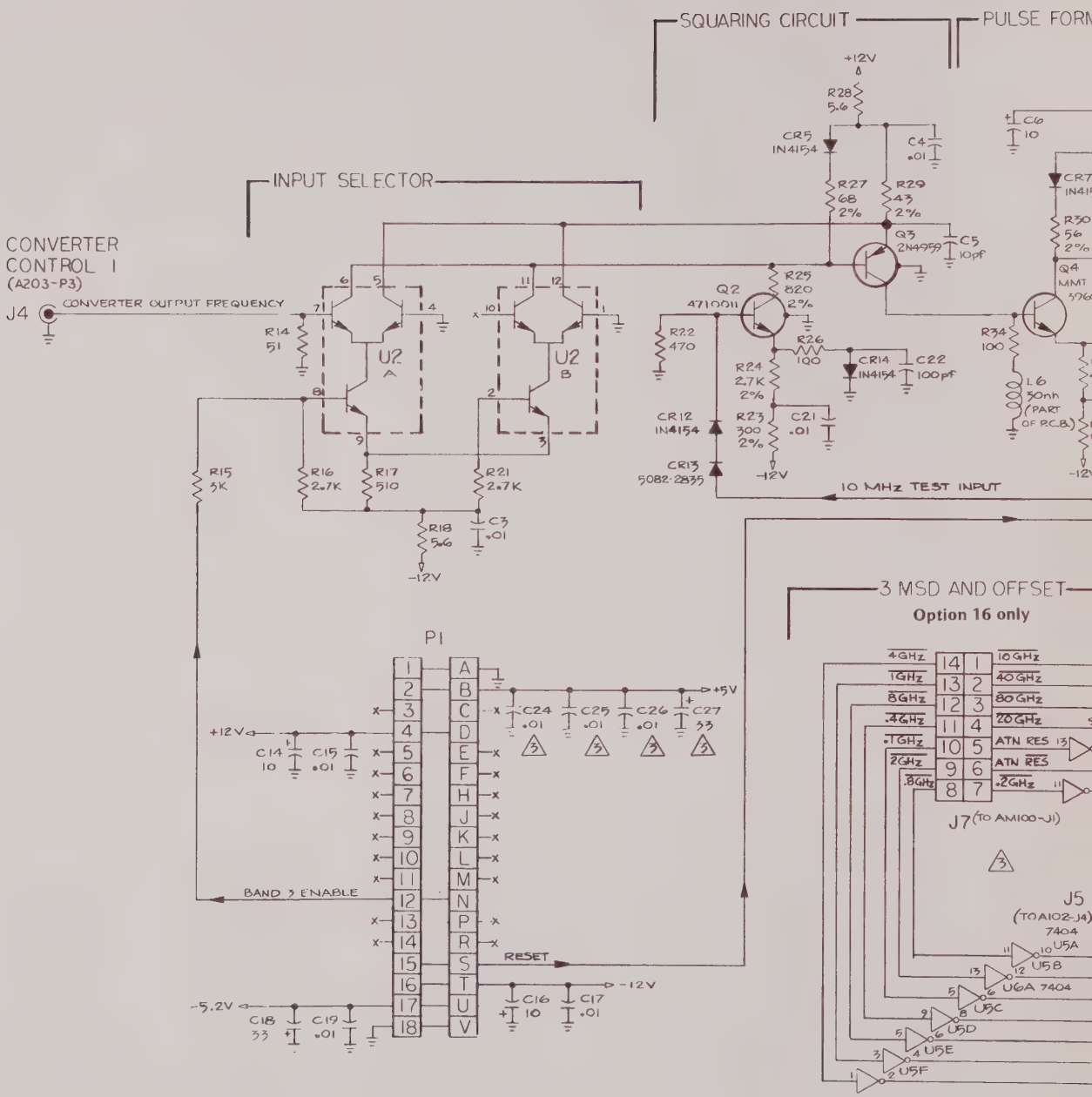
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R36	R18				
R37	Met Ox, 62 ohms, 2%	4130620	1	C4/2%/62	24546
R38	Met Ox, 47 ohms, 2%	4130470	1	C4/2%/47	24546
R39	R17				
R40	Comp, 10 ohms, 5%	4010100	1	RC07GF100J	81349
R41	Met Ox, 39 ohms, 2%	4130390	1	C4/2%/39	24546
R42	R18				
R43	Met Ox, 75 ohms, 2%	4130750	1	C4/2%/75	24546
R44	Met Ox, 560 ohms, 2%	4130561	1	C4/2%/560	24546
R45	Met Ox, S.A.T., 2%	4130999	1	C4/2%/ (1.1K Nom)	24546
R46	R35				
R47	Comp, 150 ohms, 5%	4010151	1	RC07GF151J	81349
R48	Not Used				
R49	Comp, 10K ohms, 5%	4010103	4	RC07GF103J	81349
R50	R49				
R51	R49				
R52	Comp, 680 ohms, 5%	4010681	1	RC07GF681J	81349
R53	R49				
U1	Not used				
U2	Dual Diff Ampl	3043049	1	CA3049T	0000X
U3	UHF BCD Counter	3010637	1	SP8637B	0000C
U4	Hex Inverter (Op 16 Only)	3087404	(5)	DM74LS04N	0000X
U5 thru U8	U4 (Op 16 only)				



Note: U4 thru U8
J7 and J8
Option 16 only

2020068-31 C

Figure 106a. Component Locator


SQUARING CIRCUIT
PULSE FORM
INPUT SELECTOR
CONVERTER
CONTROL I
(A203-P3)
J4
CONVERTER OUTPUT FREQUENCY
+12V
R28
5.6
CR5
IN4154
C4
.01
C6
10
R27
68
2%
R29
43
2%
Q3
2N4959
C5
10pf
R30
56
2%
Q4
MMT
R14
51
U2
A
U2
B
Q2
471001I
R25
820
2%
R22
470
R26
100
CR14
IN4154
C22
100pf
R24
2.7K
2%
R23
300
2%
C21
.01
CR12
IN4154
CR13
5082-2835
-12V
R34
100
L6
30nh
(PART
OF PCB)
10 MHz TEST INPUT
R15
5K
R16
2.7K
R17
510
R21
2.7K
R18
5.6
C3
.01
3 MSD AND OFFSET
Option 16 only
P1
+12V
C14
10
C15
.01
C24
.01
C25
.01
C26
.01
C27
33
+5V
BAND 3 ENABLE
RESET
-12V
-5.2V
C18
33
C19
.01
C16
10
C17
.01
4GHz
2GHz
1GHz
.8GHz
.4GHz
.2GHz
10GHz
40GHz
80GHz
20GHz
ATN RES
ATN RES
J7 (TO AM100-J1)
J5
(TO A102-J4)
7404
U5A
U5B
U6A 7404
U5C
U5D
U5E
U5F

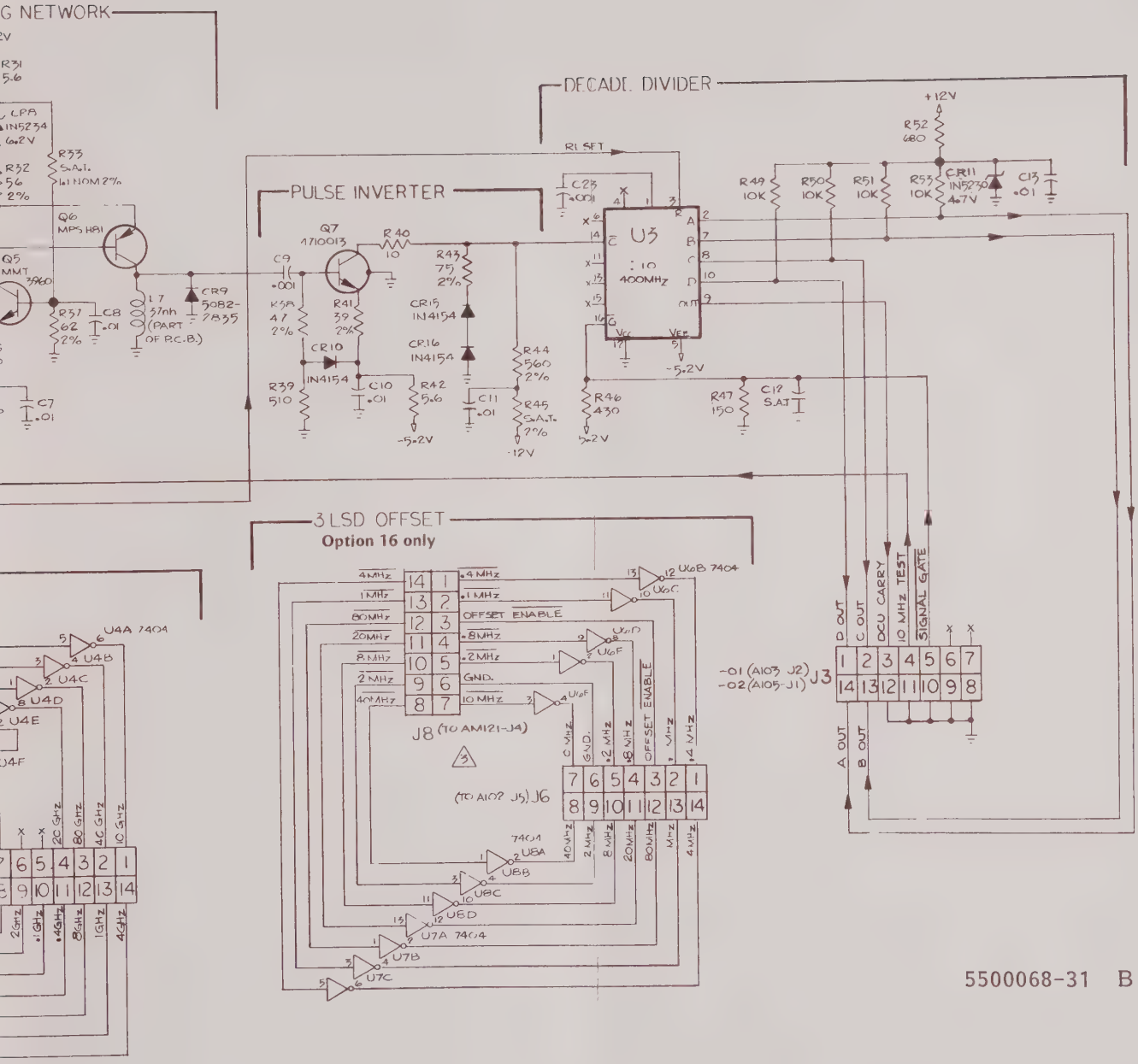


Figure 106b. Schematic Diagram

A1/A107
POWER SUPPLY

The Power Supply furnishes all basic operating voltages required by the counter. The supply consists of two assembly groups.

- PC Board A107 contains the rectifiers, filter capacitors, and regulator circuitry.
- Chassis mounted components (A1-) consist of the power transformer (T1), primary wiring, fuse (F1), 115/230 power switch (S102), and the front panel POWER On/Off Switch (S101).

CIRCUIT DESCRIPTION

The basic voltages required by the counter are unregulated +18V, regulated +12V, -12V, +5V and -5.2V.

All the regulated voltages are produced by full wave rectifier and series regulator circuits. The +18V unregulated voltage is also the input voltage for the +12V regulator.

Each of the four regulator circuits contains an integrated circuit voltage regulator with current foldback capability, protective diodes, and provision for adjustment to the required output voltage.

The type of IC used in both the +12V and +5V regulators is an LM305. This IC contains an internal temperature compensated voltage reference, as well as the necessary circuits to provide gain and current foldback limiting. The foldback current limit control resistors in the +5V supply (for example), are R11, R12, and R13.

The negative supplies utilize an LM304 as the basic IC regulator. This IC also contains an internal temperature compensated reference. To implement this reference an external pre-regulator is required. In the -12V circuit (for example), the pre-regulator includes R22, R25, and CR9. Current foldback limiting uses internal IC circuitry in addition to R17, R18, R19 and Q5.

A107 Power Supply

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A107	Power Supply	2020077	1		
C1	Elec, 8500 μF, 25V	2200010	2	91S25HA852	80031
C2	Tant, 10μF, 16V	2300010	6	TAG 20-10/16	14433
C3	Mica, 47pF, 5%, 500V	2250017	1	DM15CD470JO	72136
C4	C2				
C5	Elec, 40,000μF, 15V	2200011	1	91S15JB44	80031
C6	C2				
C7	Mica, 200pF, 5%, 500V	2250009	1	DM15CD201JO	72136
C8	Tant, 47μF, 20%, 16V	2300025	1	TAG 20-47/16	14433
C9	C2				
C10	Tant, 1.0μF, 35V	2300008	2	TAG 20-1.0/35	14433
C11	Cer, .001μF, 20%, 1KV	2150001	2	5GA-D10	56289
C12	C1				
C13	C2				
C14	C10				
C15	C11				
C16	C2				
C17	Elec, 11,000μF, 15V	2200012	1	39CS15JP113	80031
CR1 thru CR4	Rectifier	2704001	8	1N4001	04713
CR5	Bridge Rectifier	2710028	1	MDA 990-1	04713
CR6	Bridge Rectifier	2710029	1	MDA 970-1	04713
CR7	CR1				
CR8	CR1				
CR9	ZEN, 12V	2720963	2	1N963A	04713
CR10	CR1				
CR11	CR1				
CR12	CR9				
J1	6 Pin, Male	2620006	1	09-18-5061	0000A
Q1	PNP, Power	4710002	4	MJE 370	04713
Q2	NPN, Power	4710001	3	MJE 3055	04713
Q3	Q1				
Q4	NPN, Power	4705989	1	2N5989	04713
Q5	PNP, GP	4704126	2	2N4126	04713
Q6	Q1				
Q7	Q2				
Q8	Q5				

A107 Power Supply (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q9	Q1				
Q10	Q2				
R1	Comp, 68 ohms, 5%	4010680	4	RC07GF680J	81349
R2	Met Ox, 36 ohms, 2%	4130360	1	C4/2%/36	24546
R3	Met Ox, 820 ohms, 2%	4130821	2	C4/2%/820	24546
R4	WW, .66 ohms, 3%, 4W	4110012	2	RS-2	91637
R5	R3				
R6	Met Film,14.7K, 1%	4061472	1	RN55D1472F	81349
R7	Cer, Variable, 500 ohms	4250009	3	72XWR500	73189
R8	Met Film,2.26K ohms, 1%	4062261	1	RN55D2261F	81349
R9	Comp, 43 ohms	4020430	1	RC2DGF430J	81349
R10	R1				
R11	Met Ox, 20 ohms, 2%	4130200	1	C4/2%/20	24546
R12	Met Ox, 100 ohms, 2%	4130101	1	C4/2%/100	24546
R13	WW, .15 ohms, 3%, 5W	4110013	1	RS-5	91637
R14	MF, 5.62K ohms, 1%	4065621	1	RN55D5621F	81349
R15	R7				
R16	MF, 2.87K ohms, 1%	4062871	1	RN55D2871F	81349
R17	Met Ox, 12K ohms, 2%	4130123	1	C4/2%/12K	24546
R18	R4				
R19	Met Ox, 910 ohms, 2%	4130911	2	C4/2%/910	24546
R20	MF, 5.76K ohms, 1%	4065761	1	RN55D5761F	81349
R21	Cer, Variable, 1K ohms	4250003	1	72XWR1K	73138
R22	MF, 2.43K ohms, 1%	4062431	3	RN55D2431F	81349
R23	R1				
R24	Comp, 100 ohms, 5%	4010101	2	RC07GF101J	81349
R25	Comp, 1K ohms, 5%	4010102	2	RC07GF102J	81349
R26	Met Ox, 5.1K ohms, 2%	4130512	1	C4/2%/5.1K	24546
R27	WW, .5 ohms, 3%, 2W	4110004	1	RS-2B	91637
R28	R19				
R29	Comp, 910 ohms, 5%	4010911	1	RC07GF911J	81349
R30	R22				
R31	R7				
R32	R22				
R33	R1				
R34	R24				
R35	R25				
U1	Voltage Regulator	3040305	2	LM305	0000X
U2	U1				
U3	Volt Reg.	3040304	2	LM304	0000X
U4	U3				

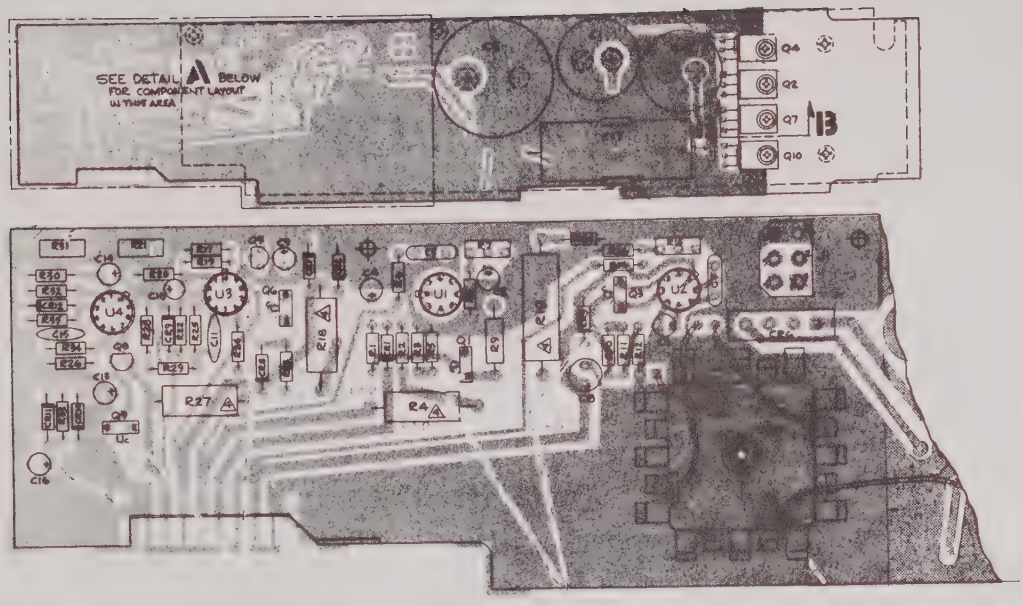
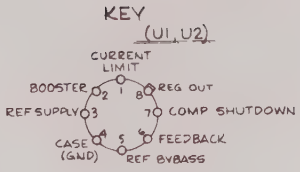
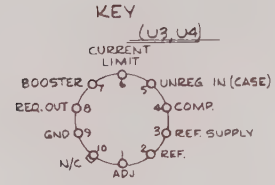
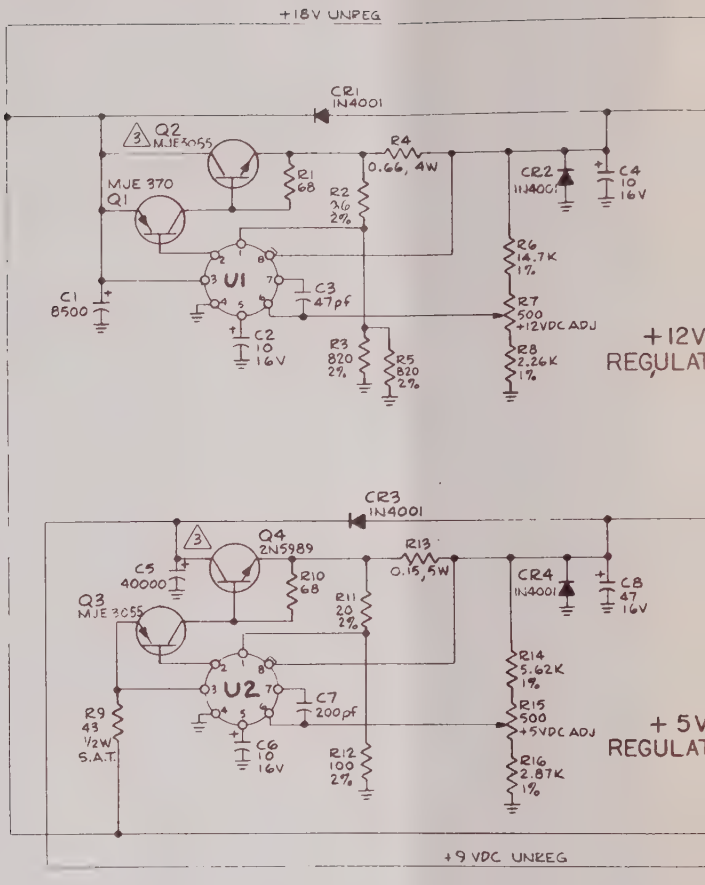


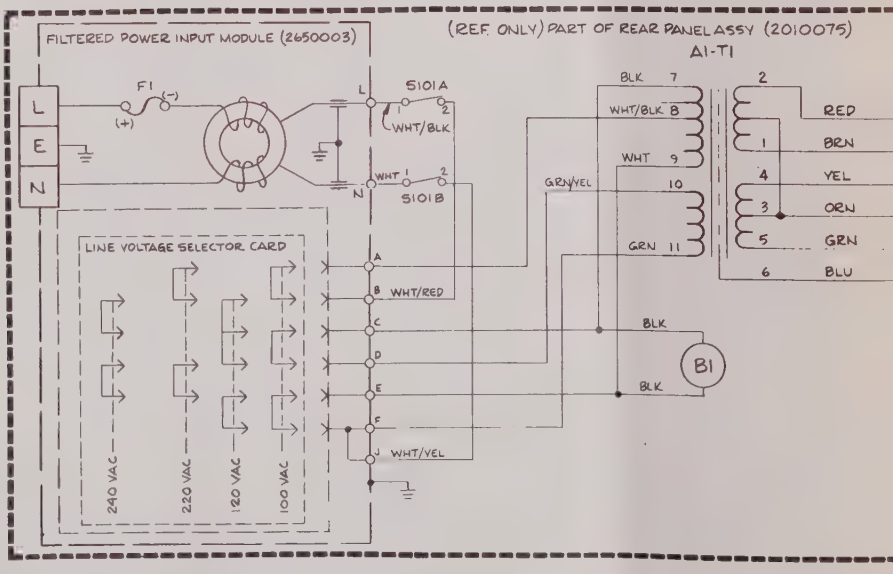
Figure 107a. Component Locator

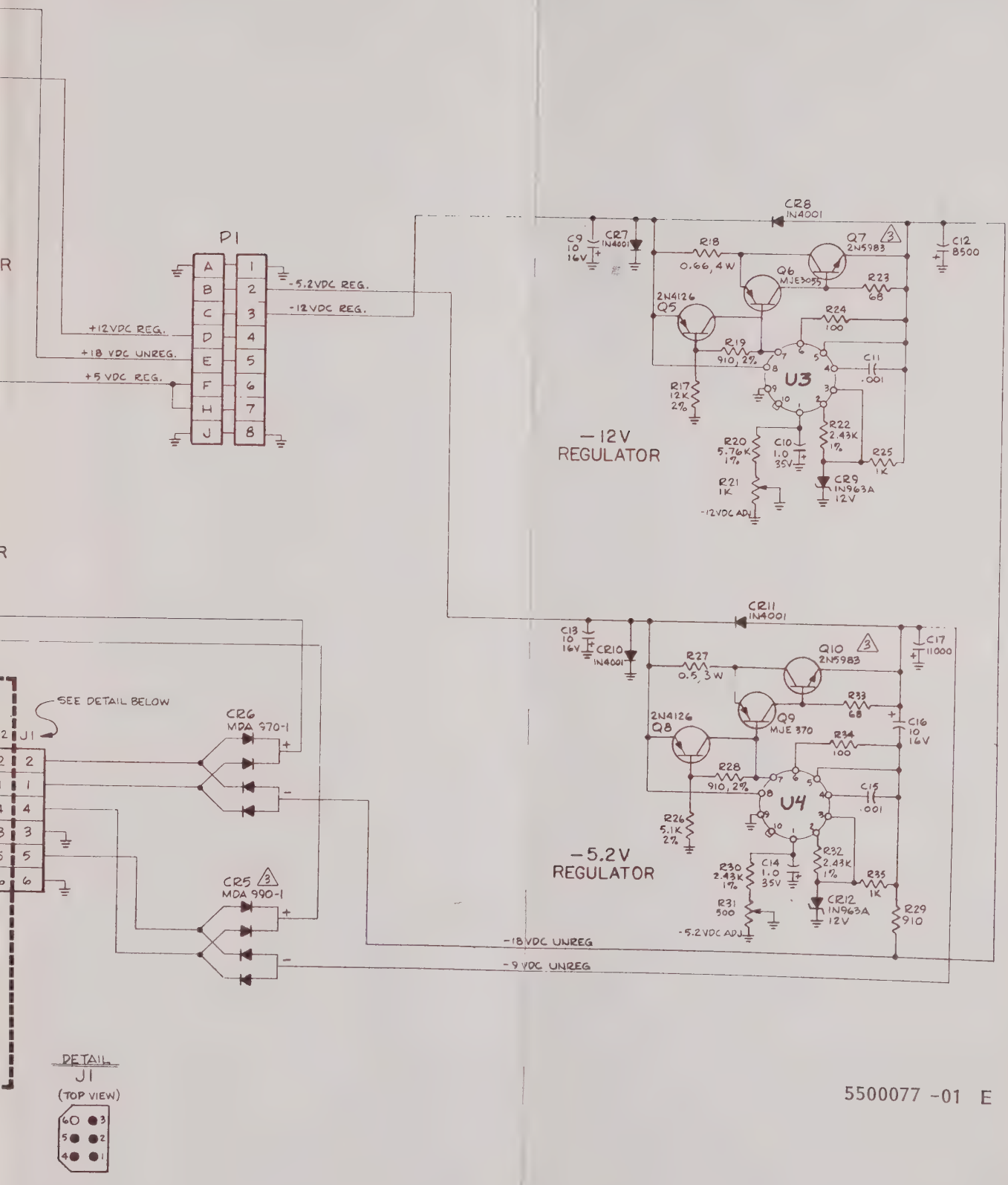
5580007


KEY
(U1, U2)
CURRENT LIMIT
BOOSTER
REG OUT
REF SUPPLY
COMP SHUTDOWN
CASE (GND)
FEEDBACK
REF BYPASS


KEY
(U3, U4)
CURRENT LIMIT
BOOSTER
UNREG IN (CASE)
REG. OUT
COMP.
GND
REF. SUPPLY
N/C
REF.
ADJ


+18V UNREG
CR1 IN4001
Q2 MJE3055
MJE 370 Q1
R1 68
R2 360 2%
R4 0.66, 4W
CR2 IN4001
C4 10 16V
R6 14.7K 1%
R7 500 +12VDC ADJ
R8 2.26K 1%
U1
C3 47pf
C1 8500
C2 10 16V
R3 820 2%
R5 820 2%
+12V REGULAT
CR3 IN4001
Q4 2N5989
Q3 MJE 3055
C5 40000
R10 68
R11 20 2%
R13 0.15, 5W
CR4 IN4001
C8 47 16V
R14 5.62K 1%
R15 500 +5VDC ADJ
R16 2.87K 1%
U2
C7 200pf
C6 10 16V
R9 43 1/2W S.A.T.
R12 100 2%
+5V REGULAT
+9 VDC UNREG


FILTERED POWER INPUT MODULE (2650003)
(REF. ONLY) PART OF REAR PANEL ASSY (2010075)
A1-T1
L
E
N
F1
S101A
S101B
WHT/BLK
WHT
LINE VOLTAGE SELECTOR CARD
240 VAC
220 VAC
120 VAC
100 VAC
WHT/RED
WHT/YEL
GRN/YEL
BLK
WHT/BLK
RED
BRN
YEL
ORN
GRN
BLU
B1



5500077 -01 E

Figure 107b. Schematic Diagram

A108
REFERENCE OSCILLATOR BUFFER

An internal temperature-compensated crystal oscillator—TCXO (A116), is used as the basic reference against which all input signals are compared. Specifications of the TCXO are listed in Section 1.

A rear panel BNC connector (A1J4) connects to A108J2 to furnish a 10 MHz square wave output signal. The power to the TCXO is switched on and off with the main counter power supply.

CIRCUIT DESCRIPTION

The TCXO sine wave is gated and converted to a TTL level in the circuit consisting of a linear, low-gain isolation amplifier Q1, a differential sine-to-square wave amplifier Q2 and Q4, and an output current driver Q5. The gate function is accomplished by switching Q3 on and off through U1. Transistors Q10-Q12, and Q13-Q15, are identical sets of gated buffer amplifiers. Buffered gain is obtained in each set by the low-gain NPN/PNP pairs Q10/Q11, and Q13/Q14. The gating function is performed by switching Q12 and Q15 on and off through U1. Q6-Q9, and Q16-Q19, are identical sets of output line drivers. Low-gain common emitter input stages Q6 and Q16 are followed by emitter followers Q7 and Q17, which drive push-pull emitter follower output pairs Q8/Q9, and Q18/Q19.

A108 Reference Oscillator Buffer

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A108	Ref Osc Buffer	2020012	1		
-A116	TCXO, Osc. XTAL	2030002	1	EIP	
C1 thru C21	Cer, .01μF, 20%, 100V	2150003	21	TG-S10	56289
CR1 thru CR5	GP, Switch	2704154	5	1N4154	07263
J1	14 Pin Socket	2630009	1	14-N-DIP	71785
J2	3Pin Conn, ML, RTA	2620029	1	09-66-1031	
J3	9 Pin Conn, ML, WAFER	2620012	1	09-18-5091	
J4	4 Pin Conn, ML, RTA	2620030	1	09-66-1041	
Q1 thru Q4	NPN	4703563	12	2N3563	07263
Q5	PNP, RF	4704258	5	2N4258	07263
Q6	Sel, 2N5179-RED	4710011	2	4705179	EIP
Q7	Q1				
Q8	Q1				
Q9	Q5				
Q10	Q1				
Q11	Q5				
Q12	Q1				
Q13	Q1				
Q14	Q5				
Q15	Q1				
Q16	Q6				
Q17	Q1				
Q18	Q1				
Q19	Q5				
R1	Comp, 8.2K ohms, 5%	4010822	6	RC07GF822J	81349
R2	Comp, 3.9K ohms, 5%	4010392	1	RC07GF392J	81349
R3	Comp, 390 ohms, 5%	4010391	1	RC07GF391J	81349
R4	Comp, 680 ohms, 5%	4010681	3	RC07GF681J	81349
R5	Comp, 2K ohms, 5%	4010202	2	RC07GF202J	81349
R6	R1				
R7	Comp, 2.2K ohms, 5%	4010222	3	RC07GF222J	81349

A108 Reference Oscillator Buffer (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R8	Comp, 750 ohms, 5%	4010751	1	RC07GF751J	81349
R9	R5				
R10	R1				
R11	Comp, 180 ohms, 5%	4010181	1	RC07GF181J	81349
R12	Comp, 27 ohms, 5%	4010270	1	RC07GF270J	81349
R13	Comp, 300 ohms, 5%	4010301	1	RC07GF301J	81349
R14	Comp, 10 ohms, 5%	4010100	4	RC07GF100J	81349
R15	R1				
R16	Comp, 4.3K ohms, 5%	4010432	2	RC07GF432J	81349
R17	R4				
R18	Comp, 560 ohms, 5%	4010561	2	RC07GF561J	81349
R19	R14				
R20	Comp, 1.1K ohms, 5%	4010112	2	RC07GF112J	81349
R21	Comp, 5.1 ohms, 5%	4010591	4	RC07GF5R1J	81349
R22	R21				
R23	Met Ox, 10K ohms, 2%	4130103	1	C4/2%/10K	24546
R24	Met Ox, 2K ohms, 2%	4130202	1	C4/2%/2K	24546
R25	Met Ox, 620 ohms, 2%	4130621	1	C4/2%/620	24546
R26	Met Ox, 300 ohms Nom, 2%	4130301	1	C4/2%/300	24546
R27	Met Ox, 430 ohms, 2%	4130431	1	C4/2%/430	24546
R28	R27				
R29	Comp, 5.1K ohms, 5%	4010512	1	RC07GF512J	81349
R30	R1				
R31	Comp, 3.6K ohms, 5%	4010362	1	RC07GF362J	81349
R32	Comp, 620 ohms, 5%	4010621	1	RC07GF621J	81349
R33	Comp, 360 ohms, 5%	4010361	1	RC07GF361J	81349
R34	Comp, 430 ohms, 5%	4010431	1	RC07GF431J	81349
R35	Met Ox, 910 ohms, 2%	4130911	1	C4/2%/910	24546
R36	R7				
R37	R14				
R38	R1				
R39	R16				
R40	R4				
R41	R18				
R42	R14				
R43	R20				
R44	R21				
R45	R21				
R46	Comp, 5.6 ohms, 5% Nom	4010596	1	RC07GF596J	81349
R46	Comp, 510 ohms, 5% Nom	4010511	1	RC07GF511J	81349
U1	Quad, NAND Gate	3087401	1	DM74LS01	

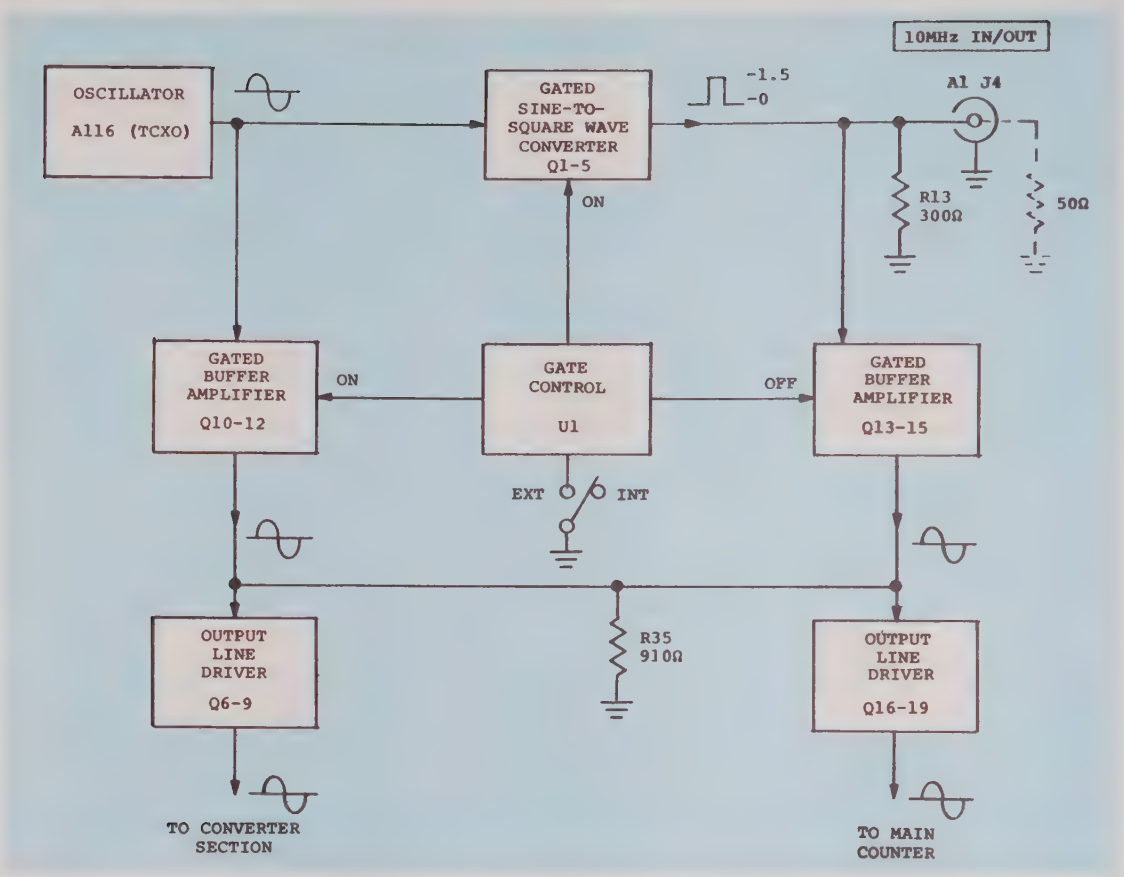


Figure 108a. Functional Diagram

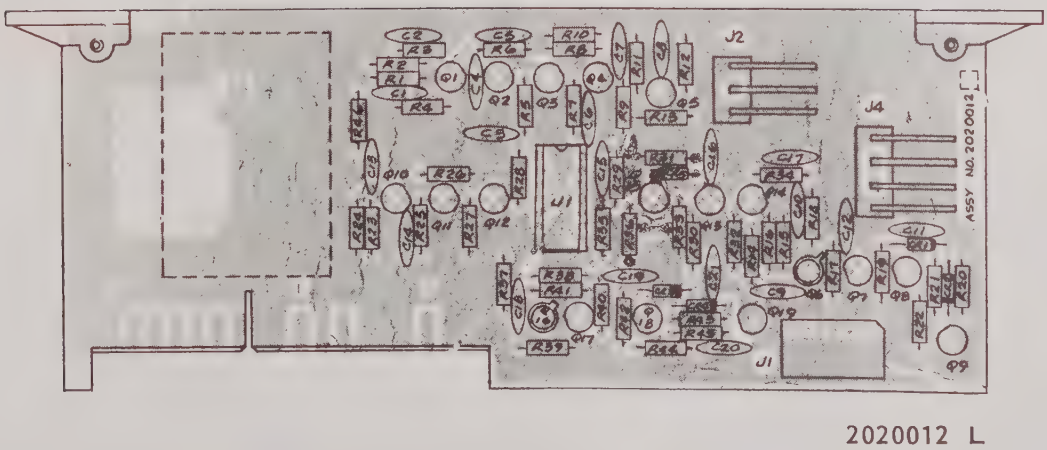
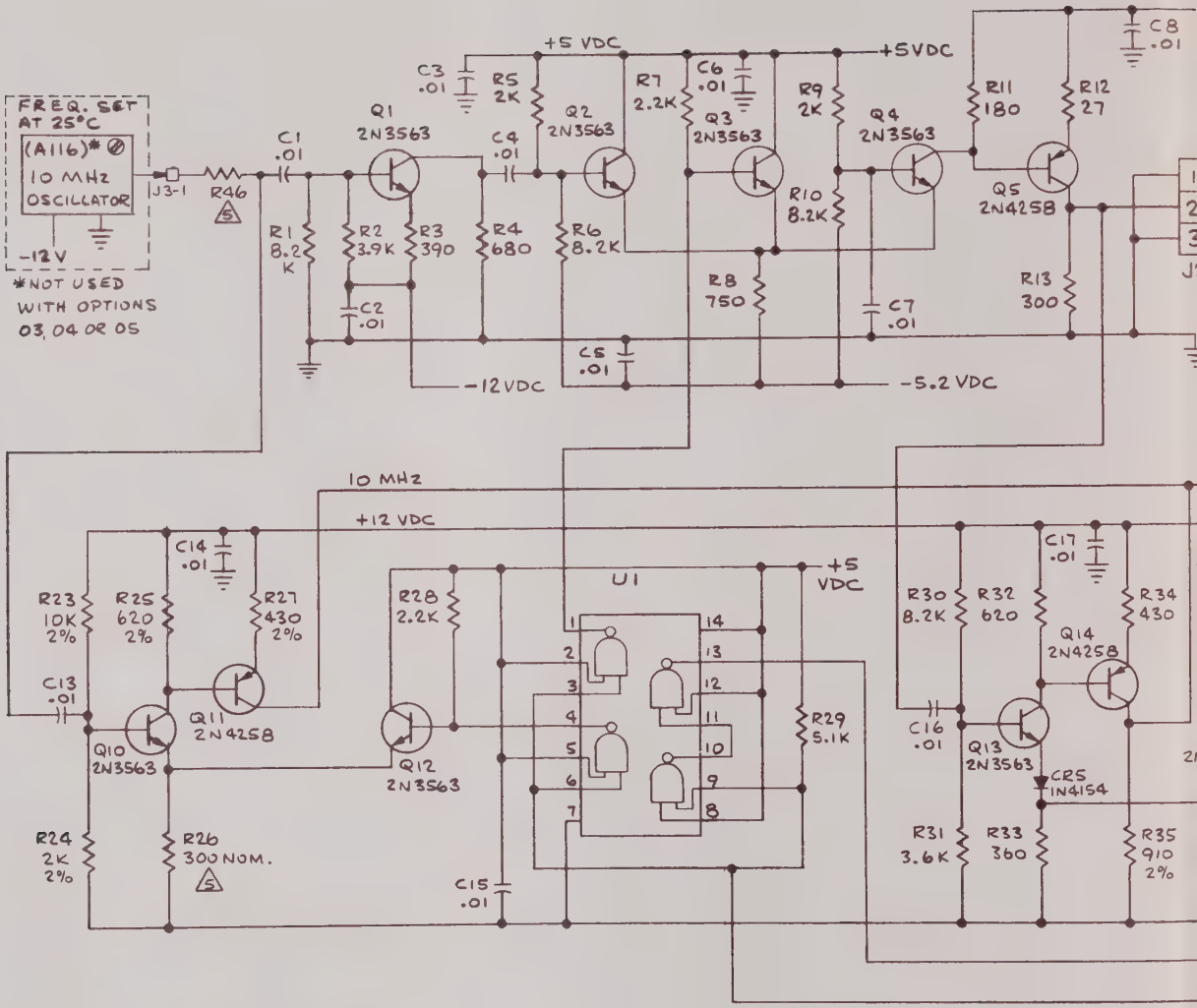


Figure 108b. Component Locator


FREQ. SET AT 25°C
(A116)*
10 MHz OSCILLATOR
-12 V
*NOT USED WITH OPTIONS 03, 04 OR 05
J3-1
R46
C1 .01
R1 8.2 K
Q1 2N3563
R2 3.9K
R3 390
C2 .01
C3 .01
R5 2K
Q2 2N3563
C4 .01
R4 680
R6 8.2K
+5 VDC
R7 2.2K
C6 .01
Q3 2N3563
R8 750
C5 .01
-12 VDC
R9 2K
Q4 2N3563
R10 8.2K
C7 .01
-5.2 VDC
+5VDC
R11 180
R12 27
Q5 2N4258
R13 300
C8 .01
10 MHz
+12 VDC
C14 .01
R23 10K 2%
R25 620 2%
R27 430 2%
C13 .01
Q11 2N4258
Q10 2N3563
R24 2K 2%
R26 300 NOM.
R28 2.2K
Q12 2N3563
U1
+5 VDC
R29 5.1K
C15 .01
R30 8.2K
R32 620
C16 .01
Q13 2N3563
C17 .01
Q14 2N4258
R34 430
CR5 IN4154
R31 3.6K
R33 360
R35 910 2%

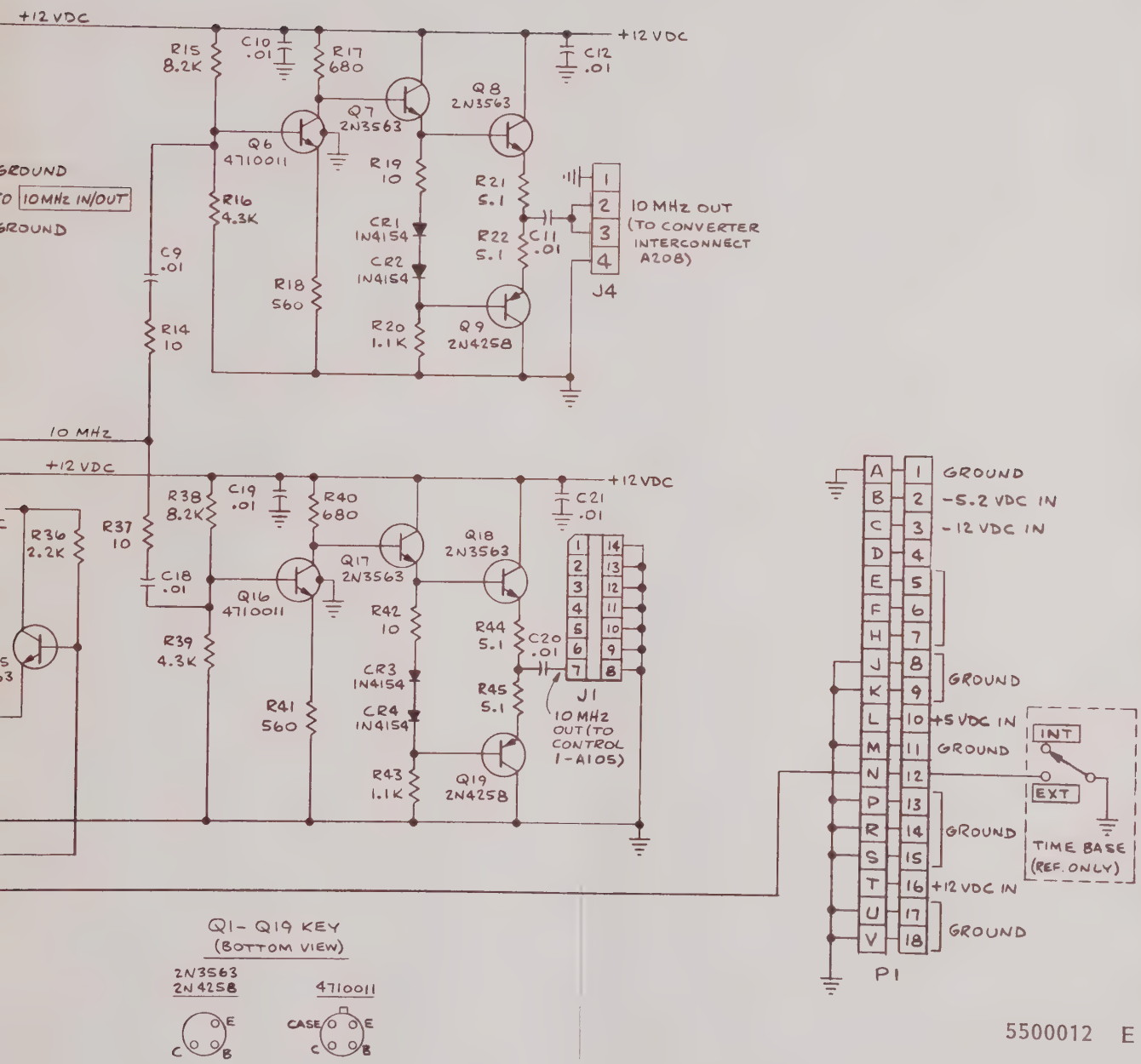


Figure 108c. Schematic Diagram

A110
DISPLAY

The Display Board (A110) contains eight LED numerical display units mounted side-by-side, with spaces between each third digit from the right. The entire assembly is mounted behind a front panel window with the digits grouped to distinctly show GHz, MHz, and kHz. All drive signals for the Display are obtained from the Count Chain Boards (A101 and A102).

The digit displays are 7-segment LED's, with the anodes of each segment tied together. When the anode is at a positive voltage, grounding any cathode through its resistor illuminates that segment.

In this multiplexed system, the anode supply is applied in pulses (through anode drivers), which are synchronized with the cathode data to determine which segment shall light.

The segment drive is applied directly to the display digits. DS1-4, DS5-7, and DS8 have their corresponding cathode segments tied together within each group.

The selector drive to groups DS1, -5, -8, and DS2-6 are each driven by two transistors in parallel to meet the higher current requirements.

The remaining LED's use single transistor drivers. The drivers saturate when turned on, applying a voltage almost equal to the supply voltage for the display. This voltage is variable (by A103R22) for display brightness adjustment.

Two display lamps are included on this assembly, which illuminate to indicate GATE operation and Converter SEARCH.

A110 Display

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A110	Display	2020004	1	EIP	
DS1 thru DS8	Numeric Indicator, RED	2800004	8	5082-7730, HP	28480
DS9 thru DS11	Not Used				
DS12	LED, Green (Gate)	2800008	1	MV5253	50522
DS13	LED, Yellow (Search)	2800014	1	MV5353	50522
J1	Cable Assy.	2040001	2	EIP	
J2	J1				
Q1 thru Q7	PNP, Ampl.	4710019	7	MPS-D55	04713
R1	Comp, 470 ohms, 5%	4010471	4	RC07GF471J	81349
R2	Comp, 1.2K, 5%	4010122	7	RC07GF122J	81349
R3	R1				
R4	R2				
R5	R1				
R6	R2				
R7	R1				
R8	R2				
R9	Comp, 330 ohms, 5%	4010331	2	RC07GF331J	81349
R10	R2				
R11	Comp, 680 ohms, 5%	4010681	2	RC07GF681J	81349
R12	R2				
R13	R11				
R14	R9				
R15	R2				

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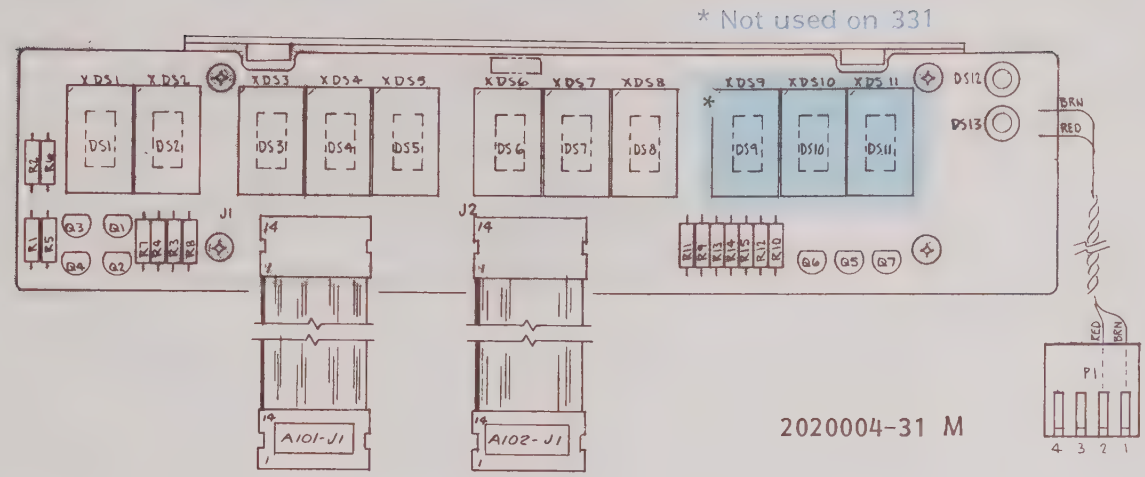
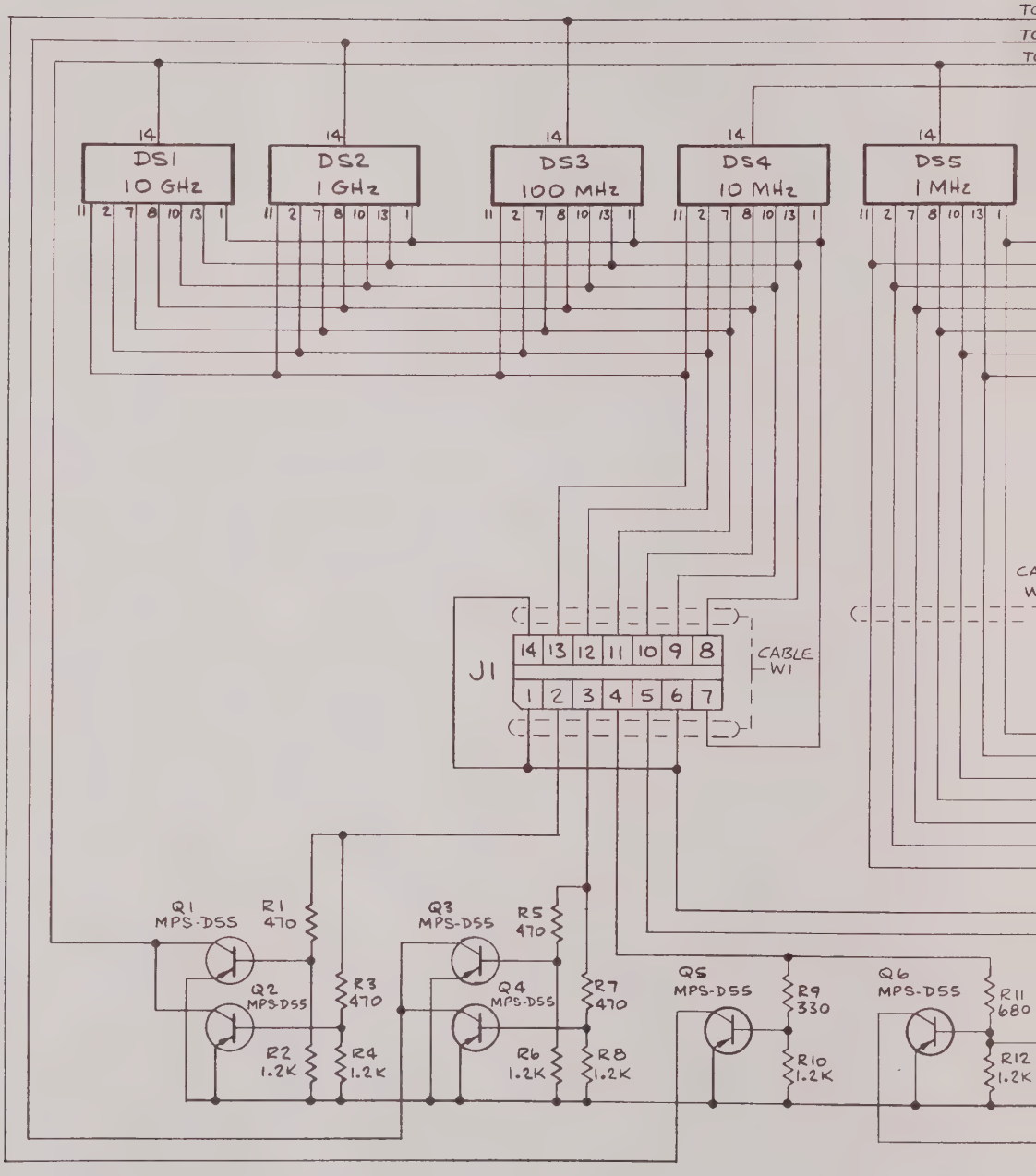


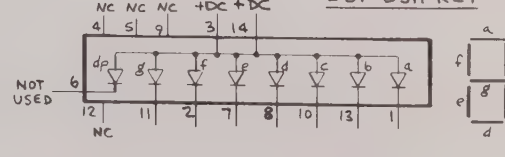
Figure 110a. Component Locator

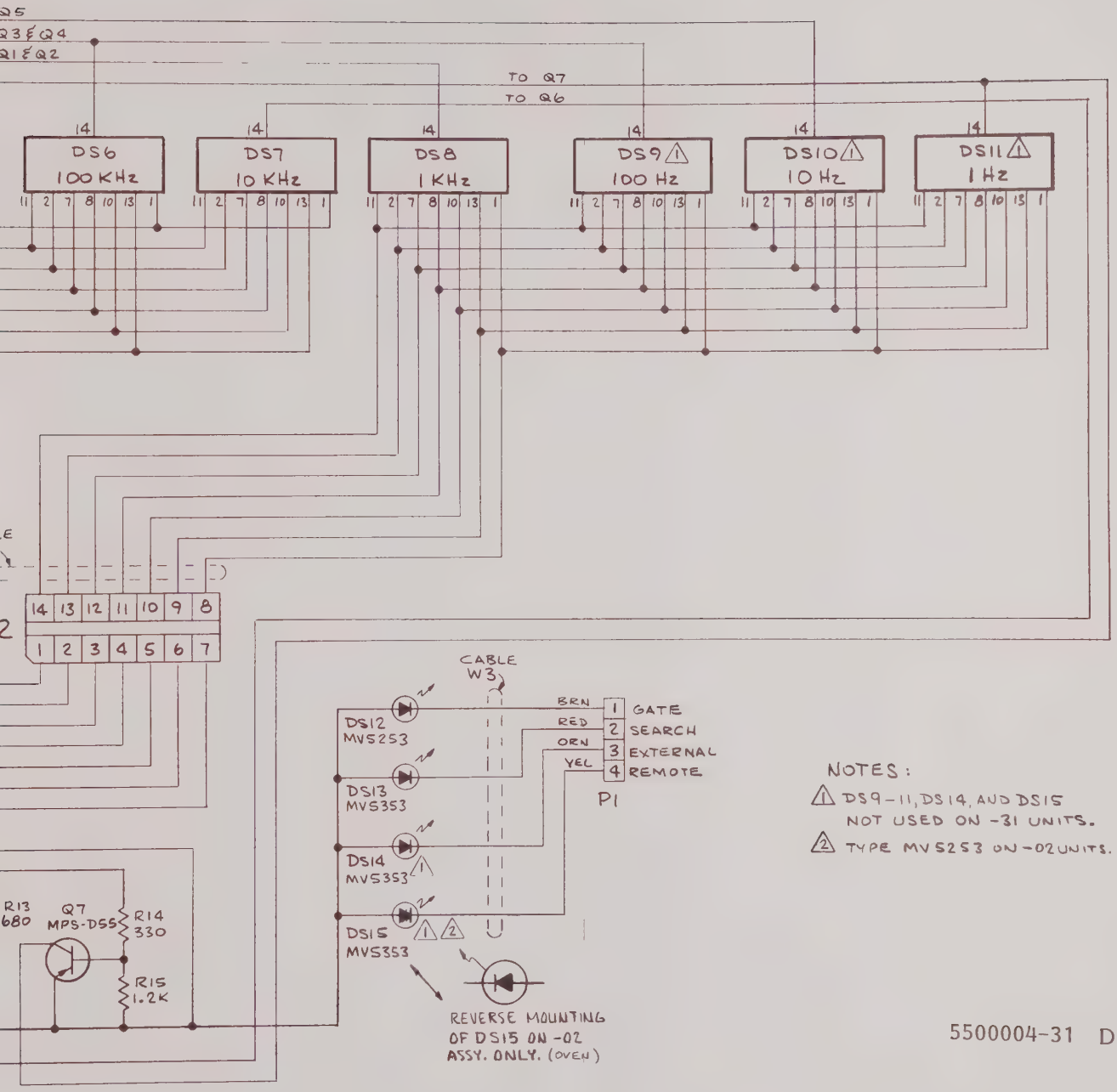


Q1-Q7 KEY

(BOTTOM VIEW)

DS1-DS11 KEY





NOTES:

1. DS9-11, DS14, AND DS15 NOT USED ON -31 UNITS.
2. TYPE MVS253 ON -02 UNITS.

5500004-31 D

Figure 110b. Schematic Diagram

A113
COUNTER INTERCONNECTION

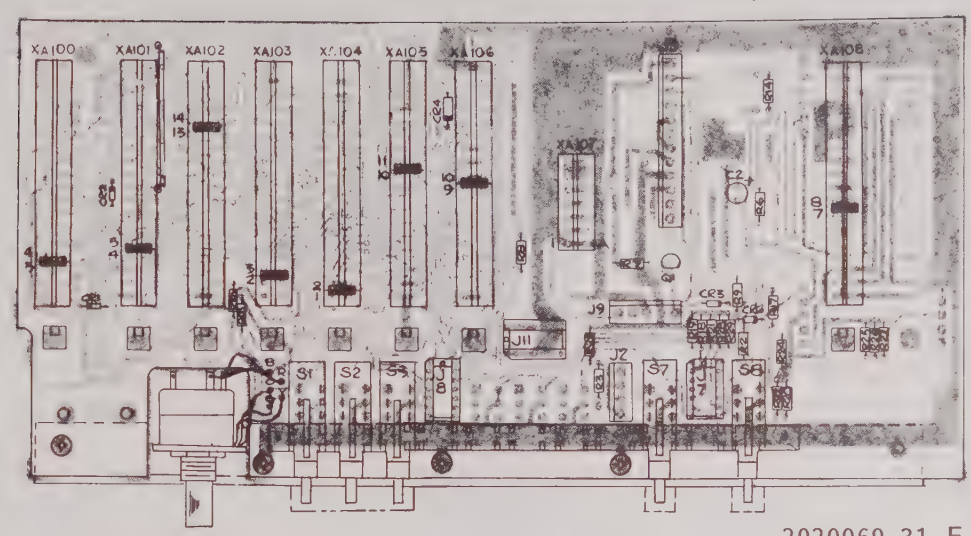
The Counter Interconnection (A113) contains the major interconnection wiring between the various counter printed circuit assemblies including both power supply distribution and signal distribution. It also contains the front panel controls of SAMPLE RATE, RESOLUTION, TEST and RESET.

A113 Counter Interconnect

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A113	Counter Interconnect	2020069			
C1	Not Used				
C2	Tant, 33μF	2300015	1	TAG 20-33/10	14433
CR1 thru CR3	GP	2704154	3	1N4154	07263
CR4		2710004	1	FH1100	07263
CR5	Not Used				
CR6		2710016	1	HP5082-2835	28480
J1	Not Used				
J2	4 Pin, Conn.	2620014	1	09-60-1041	0000A
J3	12 Pin, Conn.	2620044	1	09-60-1121	0000A
J4	5 Pin, Conn.	2620047	2	09-60-1061	0000A
J5/6	Not Used				
J7	14 Pin, Socket	2630009	3	14-N-DIP	71785
J8	J7				
J9	J4				
J10	Not Used				
J11	J7				
Q1	NPN-GP	4704124	2	2N4124	04713
Q2	PNP-GP	4704126	1	2N4126	04713
Q3	Q1				
R1	(S1) Var, 250K	4290001	1	EF8078/RVF45	11236
R2	Comp, 10 ohms, 5%	4010100	1	RC07GF100J	81349
R3	Comp, 150 ohms, 5%	4010151	1	RC07GF151J	81349
R4/5	Not Used				
R6	Comp, 75 ohms, 5%	4010750	2	RC07GF750J	81349
R7	Comp, 2.2K ohms, 5%	4010222	2	RC07GF222J	81349
R8	R7				
R9	Comp, 4.7K, 5%	4010472	1	RC07GF472J	81349
R10 thru R13	Not Used				
R14	R6				
R15	Comp, 3.3K, 5%	4010332	1	RC07GF332J	81349
R16	Comp, 1.8K, 5%	4010182	1	RC07GF182J	81349

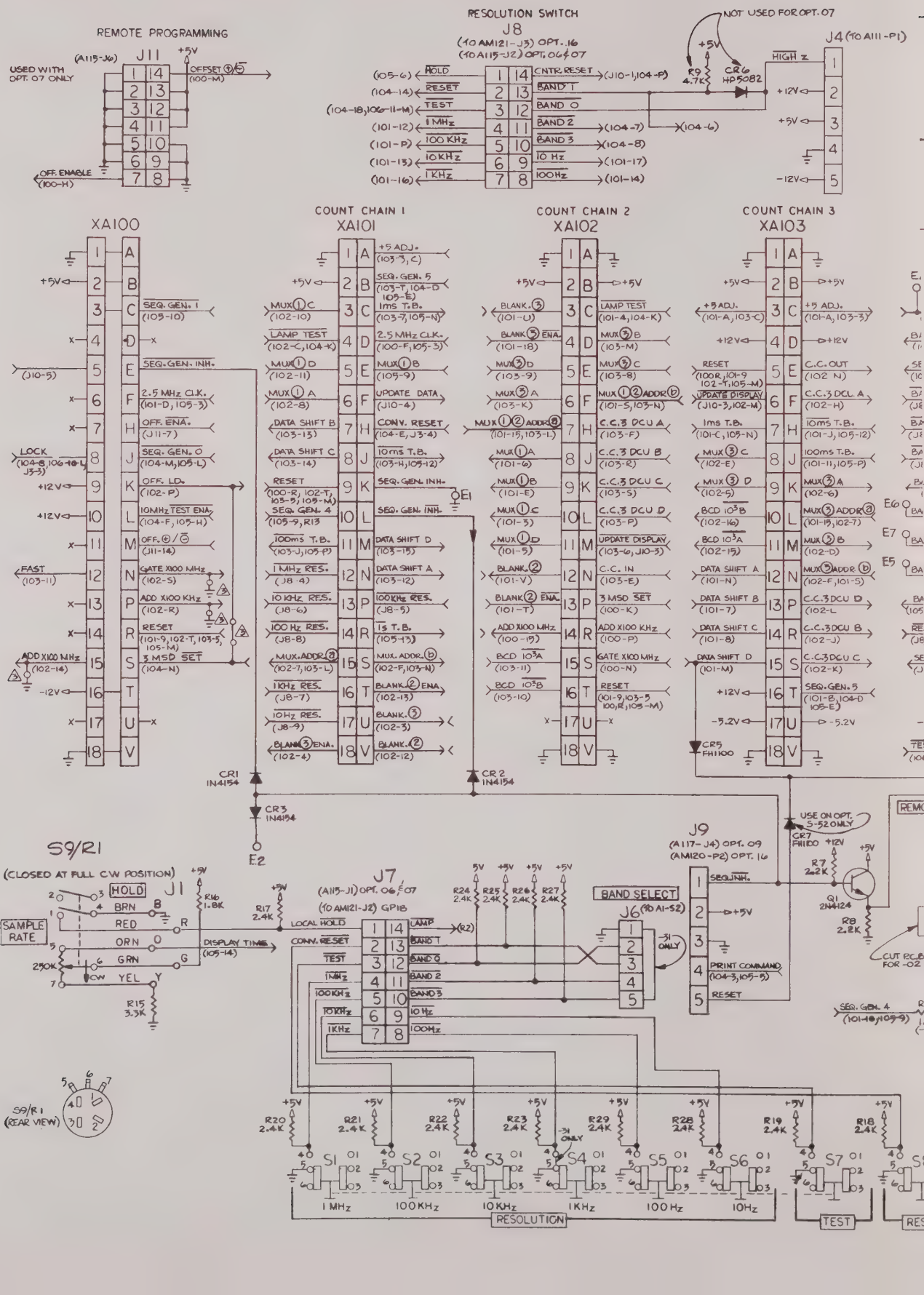
A113 Counter Interconnect (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R17 thru R29	Comp, 2.4K, 5%	4010242	13	RC07GF242J	81349
S1 thru S8	P.B., 8 Station	4500007	1	SCD/EIP	



NOTE: COMPOSITE PCB ASSEMBLY. CERTAIN COMPONENTS USED ONLY FOR SPECIFIC OPTIONS AND MODELS.

Figure 113a. Component Locator


REMOTE PROGRAMMING
J11
USED WITH OPT. 07 ONLY
OFF. ENABLE (100-H)
OFFSET (100-M)
RESOLUTION SWITCH
J8
(10 AM121-J3) OPT. 16
(10 A115-J2) OPT. 06 & 07
HOLD
RESET
TEST
1 MHz
100 KHz
10 KHz
1 KHz
CNTR. RESET
BAND 1
BAND 0
BAND 2
BAND 3
10 Hz
100 Hz
NOT USED FOR OPT. 07
R9 4.7K
CR6 HP5082
HIGH Z
J4 (TO A111-P1)
XA100
COUNT CHAIN 1
XA101
COUNT CHAIN 2
XA102
COUNT CHAIN 3
XA103
SEQ. GEN. 1
SEQ. GEN. INH.
2.5 MHz CLK.
OFF. ENA.
SEQ. GEN. 0
OFF. LD.
10MHz TEST ENA
OFF. ⊕ / ⊖
GATE X100 MHz
ADD X100 KHz
RESET
3 MSD SET
LOCK
FAST
ADD X100 MHz
-12V
+5V ADJ.
SEQ. GEN. 5
MUX ① C
1ms T.B.
LAMP TEST
2.5 MHz CLK.
MUX ① D
MUX ① B
MUX ① A
UPDATE DATA
DATA SHIFT B
CONV. RESET
DATA SHIFT C
10ms T.B.
RESET
SEQ. GEN. 4
100ms T.B.
1 MHz RES.
10 KHz RES.
100 Hz RES.
MUX. ADDR ⓐ
1KHz RES.
10Hz RES.
BLANK ③ ENA.
DATA SHIFT D
DATA SHIFT A
100KHz RES.
1s T.B.
MUX. ADDR. ⓑ
BLANK ② ENA.
BLANK ③
BLANK ②
BLANK. ③
BLANK. ②
3 MSD SET
BCD 10³B
BCD 10³A
UPDATE DISPLAY
CR5 FH1100
CR1 IN4154
CR2 IN4154
CR3 IN4154
E1
E2
S9/R1
(CLOSED AT FULL CW POSITION)
HOLD
J1
SAMPLE RATE
250K
R15 3.3K
R16 1.8K
R17 2.4K
DISPLAY TIME (105-14)
J7
(A115-J1) OPT. 06, & 07
(10 AM121-J2) GP18
LOCAL HOLD
CONV. RESET
LAMP
BAND 1
BAND 0
BAND 2
BAND 3
BAND SELECT
J6 (10 A1-S2)
-31 ONLY
R24 2.4K
R25 2.4K
R26 2.4K
R27 2.4K
J9
(A117-J4) OPT. 09
(AM120-P2) OPT. 16
SEQ. INH.
PRINT COMMAND (104-3, 105-S)
RESET
USE ON OPT. 5-52 ONLY
CR7 FH1100
R7 2.2K
R8 2.2K
Q1 2N4124
CUT PC B FOR -02
S9/R1 (REAR VIEW)
R20 2.4K
R21 2.4K
R22 2.4K
R23 2.4K
R29 2.4K
R28 2.4K
R19 2.4K
R18 2.4K
S1
S2
S3
S4
S5
S6
S7
1 MHz
100 KHz
10 KHz
1 KHz
100 Hz
10Hz
RESOLUTION
TEST

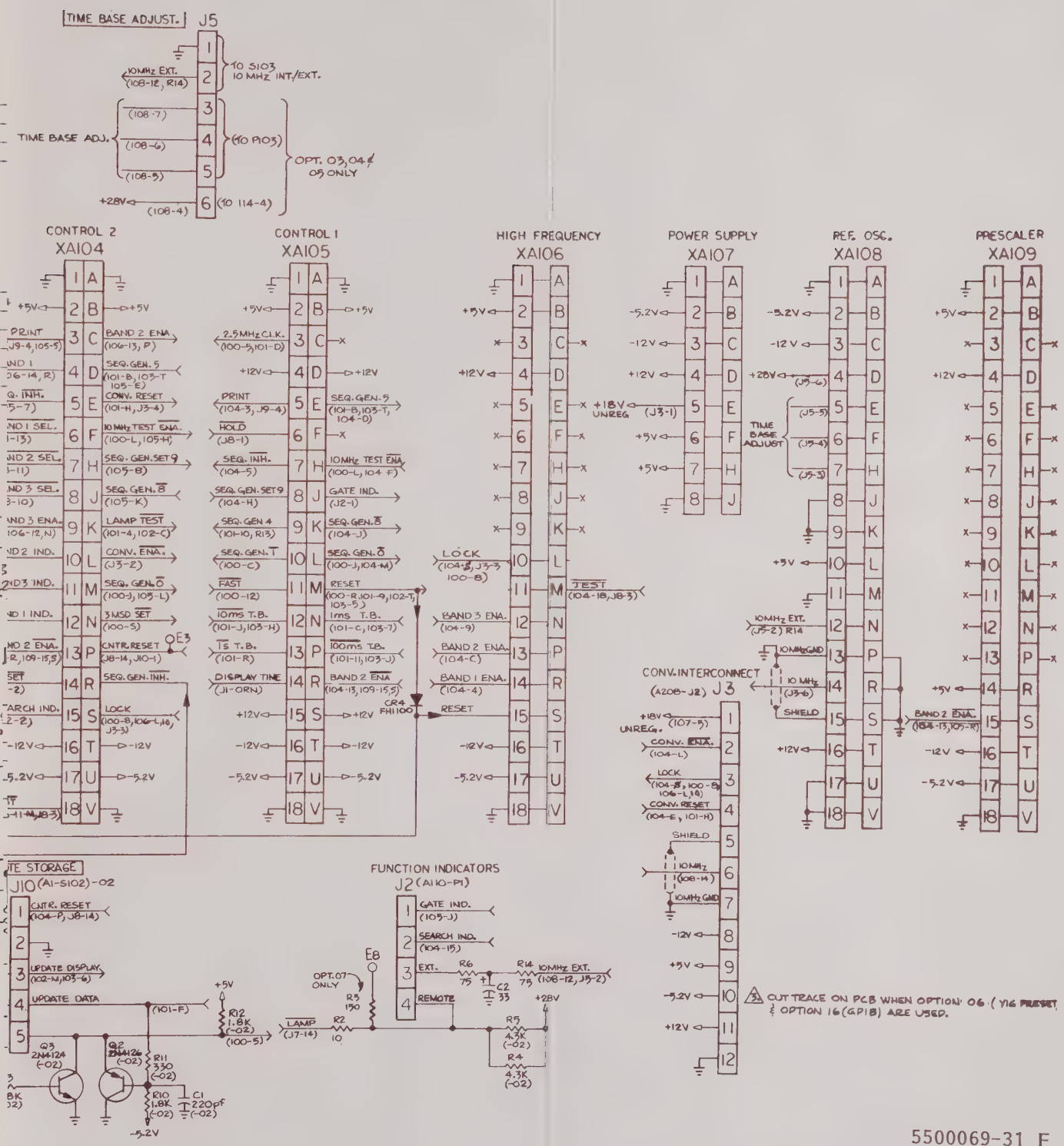


Figure 113b. Schematic Diagram

A201
SOURCE AMPLIFIER

A source of up to one watt of power at 200 MHz is required to drive the step recovery diode Comb Generator in YIG module A207. The 200 MHz must be both stable and coherent with the master oscillator in the counter. Stability is required to provide an IF spectrum that is dependent only upon the input signal spectrum. Coherence with the master oscillator is required to make counting accuracy dependent only upon the accuracy of the master oscillator.

The requirements of stability and coherence are satisfied by using a phase locked loop to lock a 200 MHz LC oscillator to the 10 MHz Time Base oscillator. The required output power is generated by a class C amplifier that contains a leveling loop to set the power output at any desired level from 1 mw to 1.1W.

CIRCUIT DESCRIPTION

The phase lock loop is a standard second order loop, implemented by using digital phase lock loop components. The 200 MHz LC oscillator is a modified Colpitts circuit with bias stabilization supplied by Q10. The output frequency of the 200 MHz oscillator is divided by 20 in U1 and U2 to produce a 10 MHz square wave. This signal is compared to the processed 10 MHz reference by phase detector U3. Phase error is amplified by active filter U4 and applied to voltage variable capacitor CR3. This holds the 200 MHz oscillator "locked" in phase to the 10 MHz reference signal. C23 sets the open loop center frequency of the oscillator.

The main power amplifier consists of four stages: Buffer amplifier Q12 and Q13, linear amplifier Q14, and two Class C stages Q15 and Q16. Output power level is controlled by adjusting the value of the negative voltage supplied by Q17 and Q18 to the linear amplifier and the Class C stages.

The power leveling loop operates by sampling the peak value of the output signal with CR5, and comparing this value to the Power Reference. The comparison is made by differential amplifier Q19 and Q20, which then controls Q17 and Q18.

A201 Source Amplifier

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A201	Source Amplifier	2020091	1	EIP	
C1	Cer, .01μF, 20%, 100V	2150003	43	TG-S10	56289
C2	C1				
C3	Tant, 1.0μF, 35V	2300008	1	TAG 20-1.0/35	14433
C4	Tant, 33μF, 10V	2300015	1	TAG 20	14433
C5	Mica, 430pF, 5%, 500V	2250032	1	DM15-431J	72136
C6	Cer, .001μF, 20%, 1KV	2150001	6	5GA-D10	56289
C7 thru C10	C1				
C11	Cer, 20pF, NPO, 500V	2160016	2	301000COG0200J	72982
C12	Cer, 18pF, NPO, 500V	2160007	1	301000COG0180J	72982
C13 thru C15	C1				
C16	Trim, 8-25pF, 250V	2350003	2	10S-T-22-8/25	0000B
C17	Cer, 4.7pF, NPO, 500V	2160013	2	301000C0H0479C	72982
C18	Cer, 15pF, NPO, 500V	2160006	2	301000C0H0150J	72982
C19	C1				
C20	Mica, 150pF, 5%, 500V	2250005	1	DM15-151J	72136
C21	C1				
C22	Cer, 12pF, NPO, 500V	2160005	3	301000C0G0120J	72982
C23	Trim, 2-8pF, 250V	2350001	1	10S-T-22-2/8	0000B
C24	Cer, 2.2pF, NPO, 500V	2160008	1	301000C0J0229J	72982
C25	Cer, 10pF, NPO, 500V	2160004	1	301000C0H0100C	72982
C26	C1				
C27	Tant, 47μF, 20%, 16V	2300025	1	TAG 20-47/16-20	14433
C28	C1				
C29	C22				
C30	C22				
C31	C11				
C32	C1				
C33	C6				
C34	C6				
C35	C16				
C36	C17				
C37	C18				
C38	C1				
C39	Mica, 100pF, 5%, 500V	2250002	4	DM15-101J	72136
C40	Trim, 5.5-18pF, 250V	2350002	3	10S-T-22-5.5/18	0000B
C41	Cer, 24pF, NPO, 500V	2160010	4	301000C0G0240J	72982
C42	C41				

A201 Source Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C43	C1				
C44	C1				
C45	C40				
C46	C41				
C47 thru C49	C1				
C50	C39				
C51	C1				
C52	C40				
C53	C41				
C54	C1				
C55	C1				
C56	Trim, 5.5-18pF, 250V	2350022	1	10S-T-24-5.5/18	0000B
C57	C39				
C58	C39				
C59 thru C61	C1				
C62	Tant, 10μF, 25%	2300029	1	TAG 20-10/25(M)	14433
C63	C6				
C64 thru C66	C1				
C67	Mica, 33pF, 5%, 500V	2250014	1	DM15CD330JO	72136
C68	Not Used				
C69 thru C80	C1				
C81	C6				
C82	C6				
C83	C1				
C84	C1				
	S-52 OPTION ONLY				
C85	Mica, 2pF, 500V	2350028	1	CD6CDO20DO3	14655
C86	C41				
C87	C40				
C88	C6				
CR1	Hot Carrier	2710006	2	5082-2800	28480
CR2	G.P.	2704154	8	1N4154	07263
CR3	Varicap	2710012	1	MV109	04713

A201 Source Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
CR4	CR2				
CR5	CR1				
CR6 thru CR11	CR2				
L1	Not Used				
L2	Not Used				
L3	Ind., 100μH	3520007	1	1537-76	99800
L4	Ind., 1μH	3510003	5	DD-1.00	72259
L5	Part of Board				
L6	Part of Board				
L7	L4				
L8	Part of Board				
L9	Part of Board				
L10	Ind., 1.2μH	3510010	17	1025-22	99800
L11	Ind., 0.1μH	3510001	1	DD-0.10	72259
L12	L4				
L13	Part of Board				
L14	L10				
L15	L10				
L16	L4				
L17	Part of Board				
L18 thru L21	L10				
L22	Ind., 0.12μH	3510011	1	DD-0.12	72259
L23	L4				
L24 thru L33	L10				
Q1	NPN, GP	4704124	3	2N4124	04713
Q2	Q1				
Q3	Graded: 2N5179 - Yel	4710012	5	EIP	
Q4	PNP, RF	4710010	2	MPS-H81	04713
Q5	Q3				
Q6	N-Channel, J-Fet	4704416	3	2N4416	04713
Q7	Q6				
Q8	Q3				
Q9	Q4				
Q10	PNP, GP	4704126	5	2N4126	04713
Q11	Graded: 2N5179 -Grn	4710013	1	EIP	

A201 Source Amplifier (Continued)

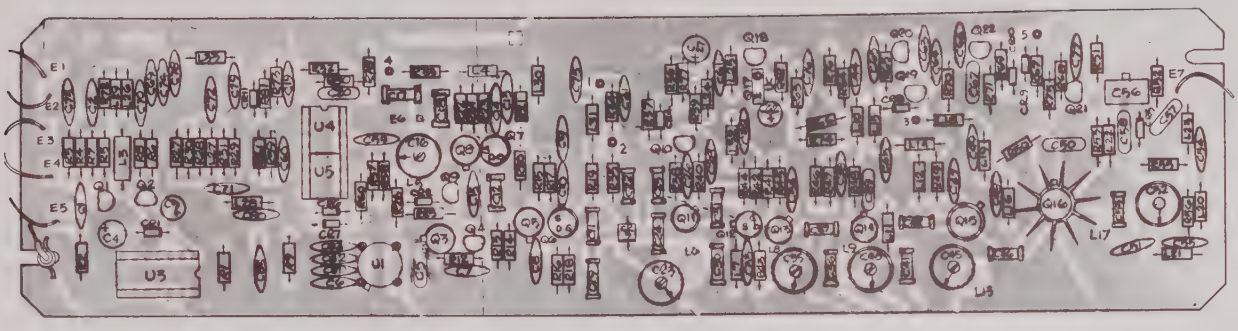
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q12	Q6				
Q13	Q3				
Q14	Q3				
Q15	NPN, RF	4720002	2	2N3866	04713
Q16	Q15				
Q17	NPN, Power	4710003	1	MJE520	04713
Q18 thru Q21	Q10				
Q22	Q1				
R1	Comp, 2.2K, 5%	4010222	1	RC07GF222J	81349
R2	Comp, 51 ohms, 5%	4010510	2	RC07GF510J	81349
R3	Met Ox, 6.8K, 2%	4130682	2	C4/2%/6.8K	24546
R4	Met Ox, 3.9K, 2%	4130392	3	C4/2%/3.9K	24546
R5	Met Ox, 270 ohms, 2%	4130271	1	C4/2%/270	24546
R6	Met Ox, 2K, 2%	4130202	1	C4/2%/2K	24546
R7	R4				
R8	R3				
R9	Met Ox, S.A.T.	4130999	3	(No. Nom. Value)	24546
R10	Not Used				
R11	Not Used				
R12	Comp, 390, 5%	4010391	1	RC07GF391J	81349
R13	Comp, 110, 5%	4010111	1	RC07GF111J	81349
R14	Met Ox, 240, 2%	4130241	1	C4/2%/240	24546
R15	Met Ox, 1.8K, 2%	4130182	2	C4/2%/1.8K	24546
R16	Met Ox, 1.2K, 2%	4130122	3	C4/2%/1.2K	24546
R17	Met Ox, 6.2K, 2%	4130622	5	C4/2%/6.2K	24546
R18	R17				
R19	Met Ox, 5.6K, 2%	4130562	1	C4/2%/5.6K	24546
R20	Met Ox, 9.1K, 2%	4130912	2	C4/2%/9.1K	24546
R21	Met Ox, 3K, 2%	4130302	3	C4/2%/3K	24546
R22	R16				
R23	Met Ox, 820, 2%	4130821	3	C4/2%/820	24546
R24	Met Ox, 1K , 2%	4130102	7	C4/2%/1K	24546
R25	Comp, 1K, 5%	4010102	1	RC07GF102J	81349
R26	Comp, 4.7K, 5%	4010472	1	RC07GF472J	81349
R27	Met Ox, 510, 2%	4130511	2	C4/2%/510	24546
R28	Met Ox, 220, 2%	4130221	2	C4/2%/220	24546
R29	R27				
R30	R15				
R31	R28				
R32	Met Ox, 3.3K, 2%	4130332	2	C4/2%/3.3K	24546

A201 Source Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R33	Met Ox, 24K, 2%	4130243	3	C4/2%/24K	24546
R34	Comp, 24K, 5%	4010243	1	RC07GF243J	81349
R35	R33				
R36	R24				
R37	Met Ox, 11K, 2%	4130113	2	C4/2%/11K	24546
R38	Comp, 39K, 5%	4010393	1	RC07GF393K	81349
R39	Met Ox, 200, 2%	4130201	2	C4/2%/200	24546
R40	R24				
R41	R20				
R42	R21				
R43	R16				
R44	R23				
R45	R24				
R46	R4				
R47	R21				
R48	R39				
R49	Met Ox, 30, 2%	4130300	1	C4/2%/30	24546
R50	R9				
R51	R17				
R52	R24				
R53	R33				
R54	Not Used				
R55	Comp, 1.1K, 2%	4130112	1	C4/2%/1.1K	24546
R56	Comp, 100 ohms, 2%	4130101	1	C4/2%/100	24546
R57	R17				
R58	R17				
R59	R24				
R60	Met Ox, 22K, 2%	4130223	1	C4/2%/22K	24546
R61	R24				
R62	Met Ox, 10K, 2%	4130103	1	C4/2%/10K	24546
R63	R37				
R64	R23				
R65	Met Ox, 2.7K, 2%	4130272	1	C4/2%/2.7K	24546
R66	Comp, 2.7K, 5%	4010272	1	RC07GF272J	81349
R67	Met Ox, 4.7K, 2%	4130472	1	C4/2%/4.7K	24546
R68	R9				
R69	R32				
R70	Comp, 100 ohms, 5%	4010101	8	RC07GF101J	81349
R71	Comp, 10K, 5%	4010103	1	RC07GF103J	81349
R72 thru R78	R70				
R79	Not Used				

A201 Source Amplifier (Continued)

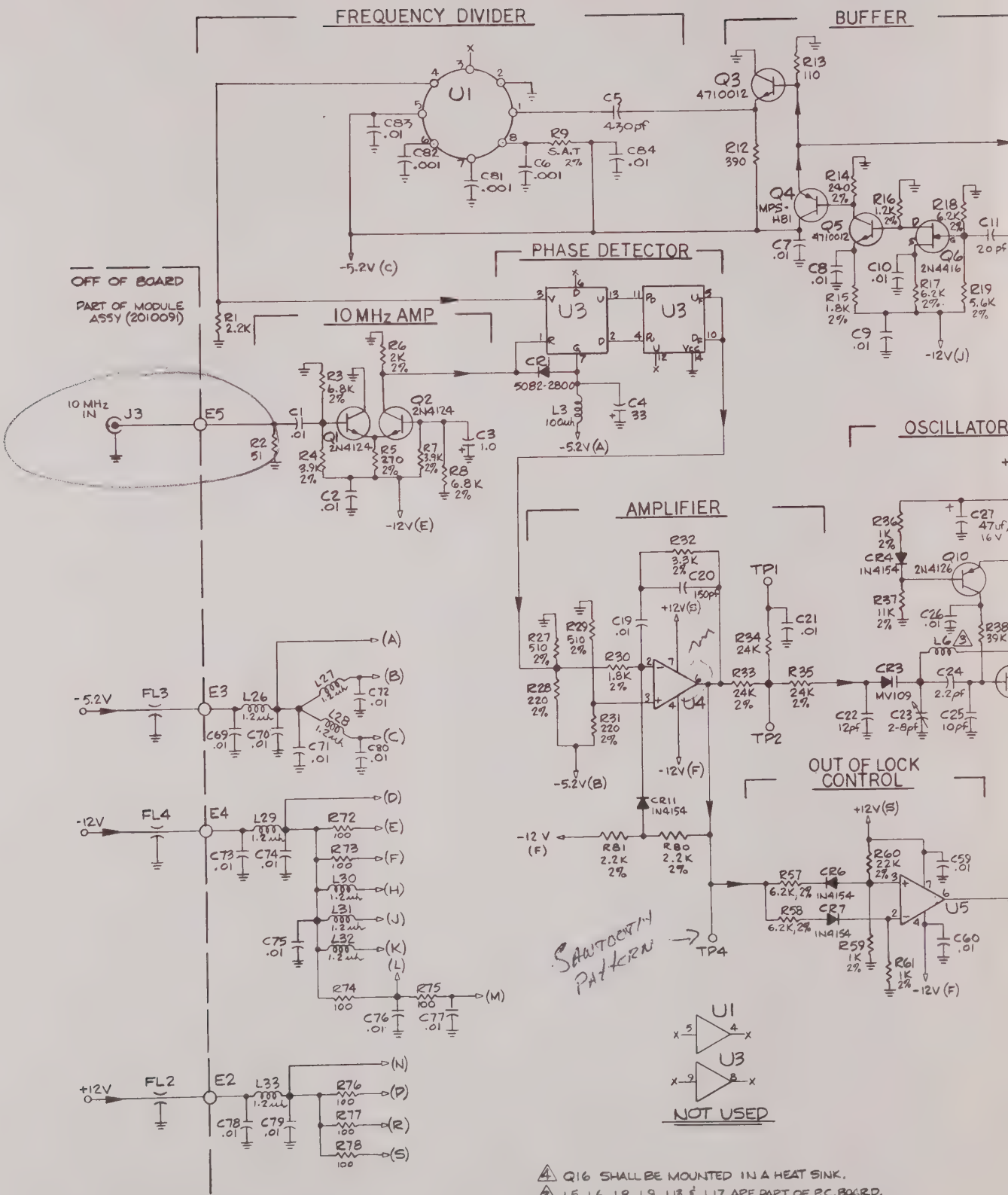
REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R80	Met Ox, 2.2K, 2%	4130222	2	C4/2%/2.2K	24546
R81	R80				
	S-52 OPTION ONLY				
R82	Met Ox, 510, 2%	4130511	1	C4/2%/510	24546
R83	Met Ox, 2.4K, 2%	4130242	1	C4/2%/2.4K	24546
R84	Met Ox, 1.6K, 2%	4130162	1	C4/2%/1.6K	24546
R85	R2				
TP1 thru TP5	Conn, Pin, .04D	2620032	5	460-2970-02-03	71279
U1	200 MHz, Hi-speed ÷ 20	3010657	1	SP8657B	Plessey
U2	Not Used				
U3	PHS/Freq. Det.	3014044	1	MC4044L	0000X
U4	Op Ampl, Low Noise	3045534	1	NE5534N	18324
U5	Op Ampl	3040741	1	741CN	0000X

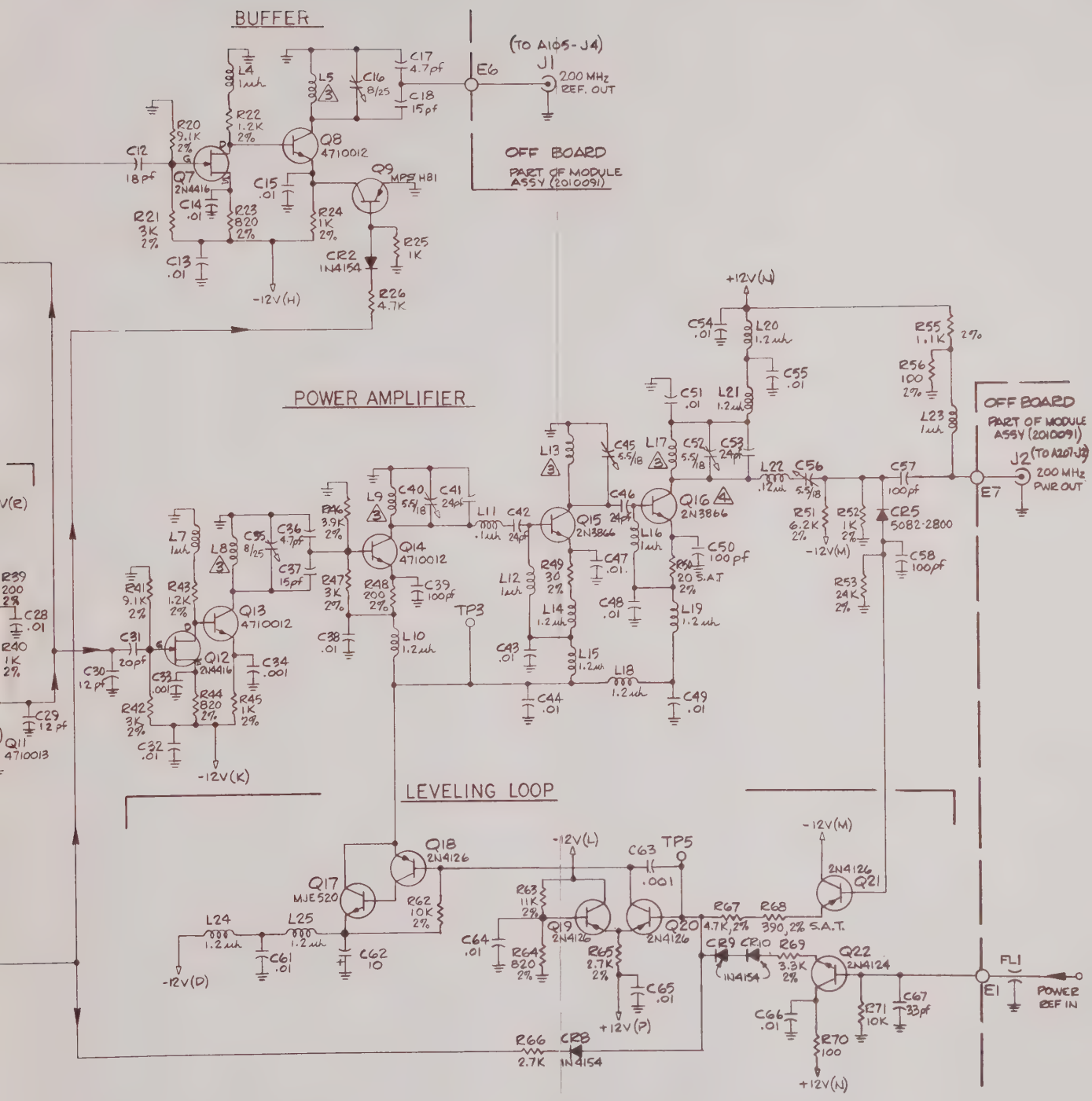


2020091 U

Figure 201a. Component Locator

5580007


FREQUENCY DIVIDER
BUFFER
PHASE DETECTOR
OFF OF BOARD
PART OF MODULE ASSY (2010091)
10 MHz AMP
OSCILLATOR
AMPLIFIER
OUT OF LOCK CONTROL
U1
U3
U4
U5
Q3 4710012
Q4 MPS-H81
Q5 4710012
Q6 2N4416
Q1 2N4124
Q2 2N4124
Q10 2N4126
CR2 5082-2800
CR3 MV109
CR4 IN4154
CR6 IN4154
CR7 IN4154
CR11 IN4154
J3
10 MHz IN
TP1
TP2
TP4
-5.2V (C)
-12V(J)
-5.2V(A)
-12V(E)
-5.2V(B)
-12V(F)
+12V(S)
-5.2V
-12V
+12V
FL3
FL4
FL2
E5
E3
E4
E2
(A)
(B)
(C)
(D)
(E)
(F)
(H)
(J)
(K)
(L)
(M)
(N)
(P)
(R)
(S)
SAWTOOTH PATTERN
NOT USED
4 Q16 SHALL BE MOUNTED IN A HEAT SINK.
5 L5, L6, L8, L9, L13 & L17 ARE PART OF P.C. BOARD.



5500091 L

Figure 201b. Schematic Diagram

A202
CONVERTER CONTROL 2

Converter Control 2 includes three circuit functions: one section comprised of two Digital-to-Analog Converters (DACs), a Sweep Driver section, and a Power Control section. The DACs provide the ramp voltage for the Sweep Driver and the three most-significant-digit presets to the counting chain. The Sweep Driver supplies the drive current to tune the YIG filter within A207. The Power Control section programs the amount of RF power delivered to the Comb Generator portion of A207.

DIGITAL-TO-ANALOG CONVERTER SECTION

This section consists of a clock generator, two digital-to-analog converters: DAC 1 and DAC 2, and logic circuits to control the clock generator and the two DACs. The DACs provide the ramp waveform that is used to control the YIG Filter. The ramp, in turn, is controlled by the clock. DAC 1 step size is 200 MHz at a rate of one step per millisecond. DAC 2 step size is 1.5 MHz at a rate of two steps per millisecond.

When the YIG Filter is locked onto a comb line, the number in DAC 1 is preset into the three most-significant-digits of the Counting Chain.

Clock pulses are generated by IC Timer U16. The NAND gates of U4 enable DAC 1 or DAC 2 and disable the clock upon command from Converter Control 1 (A203). Q11 provides a negative current step whenever DAC 2 is enabled. This compensates for the time delay between current and magnetic field within the YIG structure. This delay is the result of eddy currents generated by a changing magnetic field.

Clock pulses are converted into a ramp by successively summing in a larger amount of current each time a clock pulse occurs. One side of each summing resistor is connected to the inverting input of U3A. Each resistor will then sum in current whenever the other side of the resistor is returned to a reference voltage. For the 1.5 MHz to 100 MHz steps, the resistors are effectively connected to the +5V reference supply when their associated decade counter output goes to logic 1. For the 200 MHz to 10 GHz steps, the logic 1 outputs saturate the associated switch transistor, thus effectively connecting the resistor between the +3.1V reference supply and the U3A input. The amount of current added is carefully regulated by the tight tolerance of the summing resistors, and the temperature compensated reference voltage supplied by CR1 and U2B.

DAC 1 controls the steps from 200 MHz to 19.8 GHz; DAC 2 from 1.5 MHz to 200 MHz. U1 generates a reset pulse when DAC 2 reaches 200 MHz; U9 will generate a reset pulse when DAC 1 reaches 20 GHz. The three most-significant-digit (3MSD) information is sent to Count Chain 2 (A102) via connector J2. Connector J1 provides inputs to YIG Preset Options 31 and 32 (see Appendix B), which initiate the ramp starting point at a non-zero frequency.

SWEEP DRIVER SECTION

The Sweep Driver section consists of an operational amplifier, a voltage translator, and two cascaded output transistors. The second output transistor(A2 Q1) is mounted on the Converter chassis.

The ramp from the DACs drives the inverting input of U3B. R72 sets the ramp offset, while R70 determines the slope of the ramp. Feedback voltage is obtained across sense resistor R75, forcing an extremely linear relationship between the sweep voltage and the YIG filter current. CR3 limits the voltage developed across the YIG filter tuning coil during flyback, in order to protect transistors Q10 and A2Q1.

POWER CONTROL SECTION

The Power Control circuit provides the means for reducing the power output of the Comb Generator during the sweep period from 1 to 9.8 GHz. This limits the maximum amplitude of spurious signals generated in the Mixer. This power reduction is accomplished by varying the output level of the Source/Amplifier (A201) with the control voltage produced by the Power Control Section.

The digital information which controls DAC 1 is fed to U10, U13, and U17. U11D, U11E, and U12 are used to level the 0.8 GHz comb line. U13 divides the lines from 1 to 9.8 GHz into 1 GHz steps (five lines each). In addition, U13 is used to divide the five lines from 1 to 1.8 GHz into steps of two and three lines. U13 also makes it possible to divide up to five additional steps if necessary. U17 provides the ability to level up to five steps above 10 GHz (1 GHz per step) if necessary. By proper adjustment of each step, the power into the Comb Generator can be programmed to provide relatively constant comb line power at the Mixer diode.

A202 Converter Control 2

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A202-	Converter Control 2	2020067	1	EIP	
C1 thru C3	Cer, .01μF	2150003	7	TG-S10	56289
C4	Cer, .005μF, 20%, 100V	2150008	1	TG-D50	56289
C5	Cer, .001μF, 20%, 1KV	2150001	2	5GA-D10	56289
C6	Tant, .10μF, 35V	2300020	1	TAG 20-0.10/35	14433
C7	C1				
C8	Tant, 1.0μF, 35V	2300008	1	TAG 20-1.0/35-50	14433
C9	C5				
C10	C1				
C11	Tant, 10μF, 25V	2300029	3	TAG 20-10/25M	14433
C12	Mica, 1000pF, 5%, 500V	2250003	1	DM15CD102JO	72136
C13	C1				
C14	C1				
C15	C11				
C16	C1				
C17	Tant, 33μF, 10V	2300015	1	TAG 20-33/10-50	04713
CR1	ZNR, 6.2V, 5%	2700827	1	1N827	04713
CR2	Gen Purp.	2704154	4	1N4154	07263
CR3	ZNR, 51V	2704757	1	1N4757	04713
CR4	Rectifier	2704001	1	1N4001	04713
CR5 thru CR7	CR2				
J1	Socket, 14 pin, 1C	2630009	2	14-N-DIP	71785
J2	J1				
J3	Conn, 7 pin	2630031	1	09-66-1071	71785
Q1 thru Q8	NPN	4704401	11	2N4401	04713
Q9	NPN	4704124	1	2N4124	04713
Q10	PNP, Ampl	4710018	1	MPS-L51	04713
Q11	PNP	4704126	1	2N4126	04713
Q12 thru Q14	Q1				

A202 Converter Control 2 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R1 thru R7	Comp, 5.1K, 5%	4010512	7	RC07GF512J	81349
R8	Comp, 82M, 5%	4010826	1	RC07GF826J	81349
R9	Comp, 39M, 5%	4010396	1	RC07GF396J	81349
R10	Comp, 20M, 5%	4010206	1	RC07GF206J	81349
R11	Cmt Flm, 10M, 1%	4120018	1	CC1005F	01121
R12	Cmt Flm, 4.99M, 1%	4120017	1	CC4994F	01121
R13	Cmt Flm, 2.49M, 1%	4120016	2	CC2494F	01121
R14	Cmt Flm, 1.24M, 1%	4120015	1	CC1244F	01121
R15	Prec., 200K, 1%	4052003	1	RN55C2003F	81349
R16	Var, 10K	4250006	1	72XWR10K	73138
R17	Comp, 2.2K, 5%	4010272	7	RC07GF272J	81349
R18	Prec, 400K, .5%	4104003	1	AME55-C1-4003D	14298
R19	Comp, 10K, 5%	4010103	7	RC07GF103J	81349
R20	R17				
R21	Prec, 200K, .25%	4102003	1	AME55-C3-2003C	14298
R22	R19				
R23	R17				
R24	Prec, 100K, .1%	4101003	1	AME55-C3-1003B	14298
R25	R19				
R26	R17				
R27	Prec, 80K, .1%	4108002	1	AME55-C3-8002B	14298
R28	R19				
R29	R17				
R30	Prec, WW, 40K, .05%	4140033	1	4S8P1S8	05591
R31	Comp, 12K, 5%	4010123	2	RC07GF123J	81349
R32	R17				
R33	Prec, WW, 20K, .025%	4140032	1	447P/20K/.025%	05591
R34	Comp, 20K, 5%	4010203	2	RC07GF203J	81349
R35	R17				
R36	Prec, WW, 10K, .01%	4140031	1	447P/10K/.01%	05591
R37	Comp, 1.2K, 5%	4010122	1	RC07GF122J	81349
R38	Prec, WW, 8K, .01%	4140030	1	447P/8K/.01%	05591
R39	Prec, 750 ohms, 1%	4057500	1	RN55C7500F	81349
R40	Prec, WW, 8K, .1%	4140035	2	447P/8K/.1%	05591
R41	R40				
R42	Met Ox, 18K, 2%	4130183	1	C4/2%/18K	24546
R43	Met Ox, 11K, 2%	4130113	1	C4/2%/11K	24546
R44	R19				
R45	Comp, 3.3K, 5%	4010332	1	RC07GF332J	81349
R46	R31				
R47	Comp, 560K, 5%	4010564	2	RC07GF564J	81349

A202 Converter Control 2 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R48	R47				
R49	Var. Cer, 5K	4250005	11	72XWR5K	73138
R50 thru R57	R49				
R58	Met Ox, 20K, 2%	4130203	14	C4/2%/20K	24546
R59 thru R66	R58				
R67	R58				
R67	Comp, 1.5K, 5%	4010152	1	RC07GF152J	81349
R68	Prec, WW, 3K, .1%	4040034	2	447P/3K/.1%	05591
R69	Prec, WW, S.A.T.	4140999	1	447P/3.7K/.1%	05591
R70	Var, WW, 500 ohms	4280009	1	89PR-500	73138
R71	Prec, 49.9K, 1%	4054992	1	RN55C4992F	81349
R72	Var, Cer, 1K	4250003	1	72XWR1K	73138
R73	Prec, 39.2K, 1%	4053922	1	RN55C3922F	81349
R74	R68				
R75	WW, PWR, 5 ohms, 1%, 7W	4110003	1	T-7 (10 PPM)	12436
R76	Comp, 1.6K, 5%	4010162	1	RC07GF162J	81349
R77	Comp, 390 ohms, 5%	4010391	2	RC07GF391J	81349
R78	R77				
R79	Comp, 1K, 5%	4010102	2	RC07GF102J	81349
R80	R79				
R81	Comp, 620K, 5%	4010624	1	RC07GF624J	81349
R82	R34				
R83 thru R85	S.A.T.				
R86	R49				
R87	S.A.T.				
R88	S.A.T.				
R89	R49				
R90 thru R92	S.A.T.				
R93	R58				
R94	S.A.T.				
R95	S.A.T.				
R96	R58				
R97	R58				
R98	Comp, 7.5K, 5%	4010752	1	RC07GF752J	81349
R99	Comp, 47K, 5%	4010473	1	RC07GF473J	81349

A202 Converter Control 2 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R100	R58				
R101	Comp, 4.7K, 5%	4010472	2	RC07GF472J	81349
R102	R19				
R103	Met Ox, 8.2K, 2%	4130822	2	C4/2%/8.2K	24546
R104	Met Ox, 2.4K, 2%	4130242	2	C4/2%/2.4K	24546
R105	R103				
R106	R104				
R107	Prec, 13.3K, 1%	4051332	1	RN55C1332F	81349
R108	R58				
R109	Comp, 2K, 5%	4010202	1	RC07GF202J	81349
R110	R101				
R111	R19				
R112 thru R121	S.A.T.				
R122	R13				
TP1 thru TP6	Conn, Pin, Gold, .040D	2620032	6	460-2970-02-03	71279
U1	Dual Binary Counter	3084393	1	SN74LS393	0000X
U2	OP Amplifier	3041458	4	MC1458P1	0000X
U3	U2				
U4	2 Input NAND Gate	3087400	1	DM74LS00	0000X
U5	Hex Inverter	3087404	3	DM74LS04	0000X
U6	U5				
U7	Decade Counter	3074176	3	DM74176N	0000X
U8	U7				
U9	U7				
U10	BCD, Decimal Decoder	3087442	2	DM74LS42	0000X
U11	U5				
U12	2 Input NOR Gate	3087402	1	DM74LS02	0000X
U13	Hex Buffer	3008097	1	DM8097N	0000X
U14	U2				
U15	U2				
U16	Timer	3040555	1	NE555V	0000X
U17	U10				

5580007

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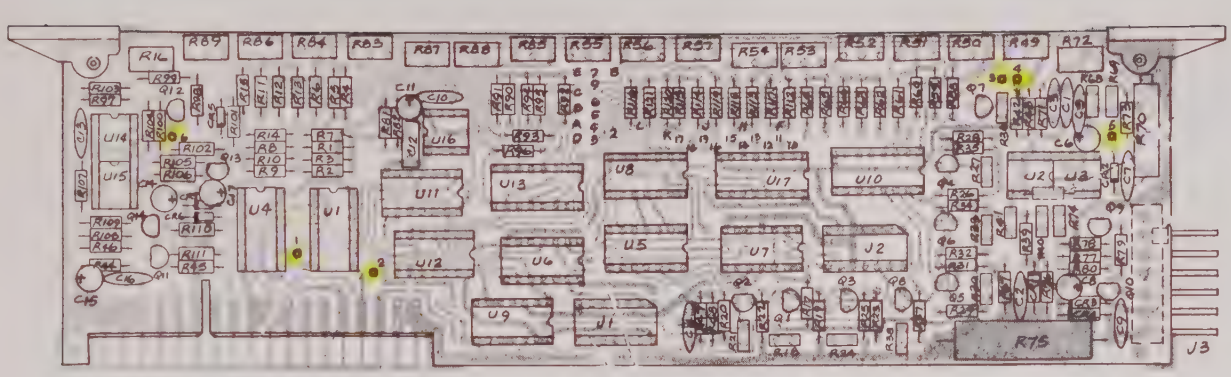
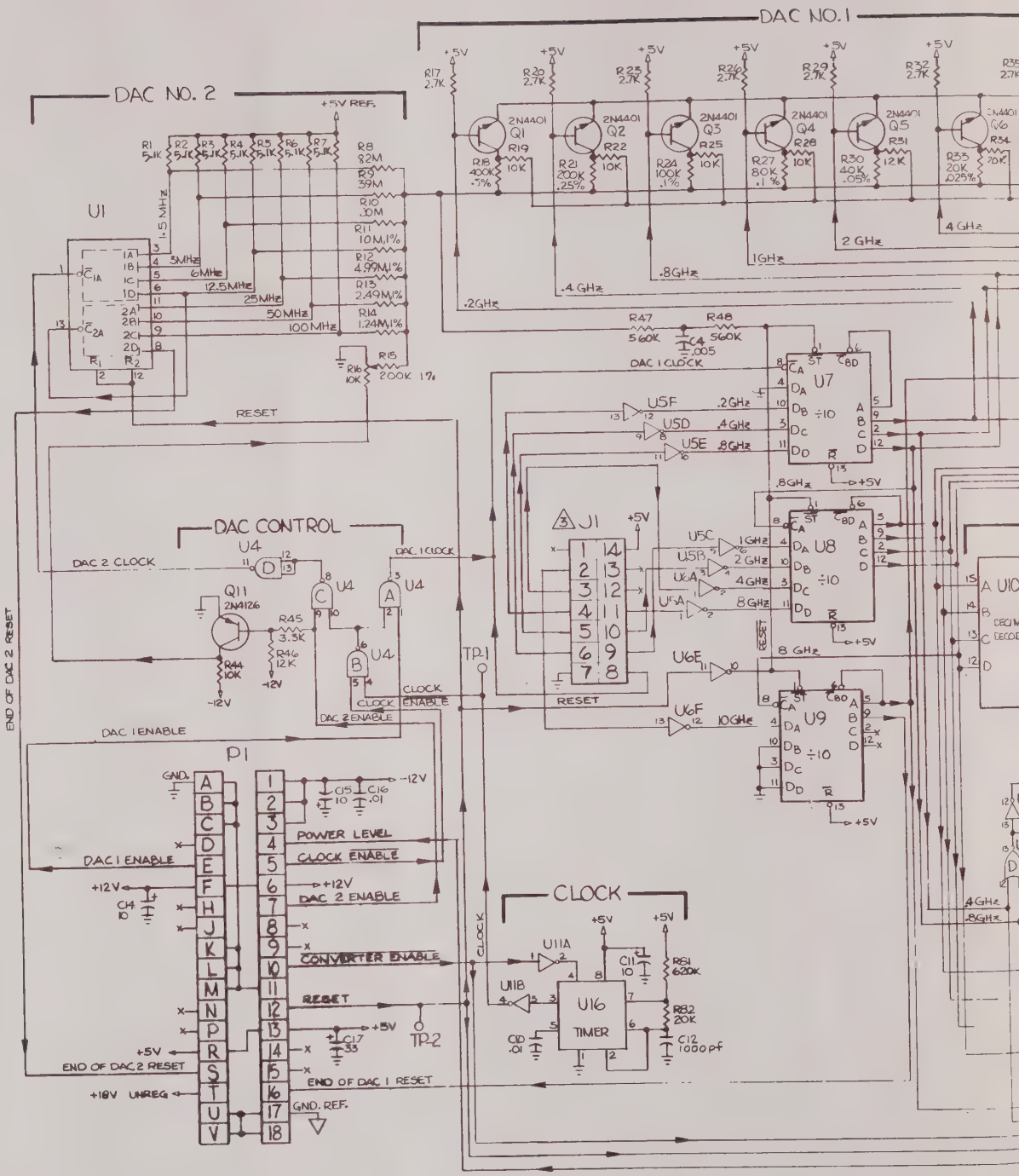


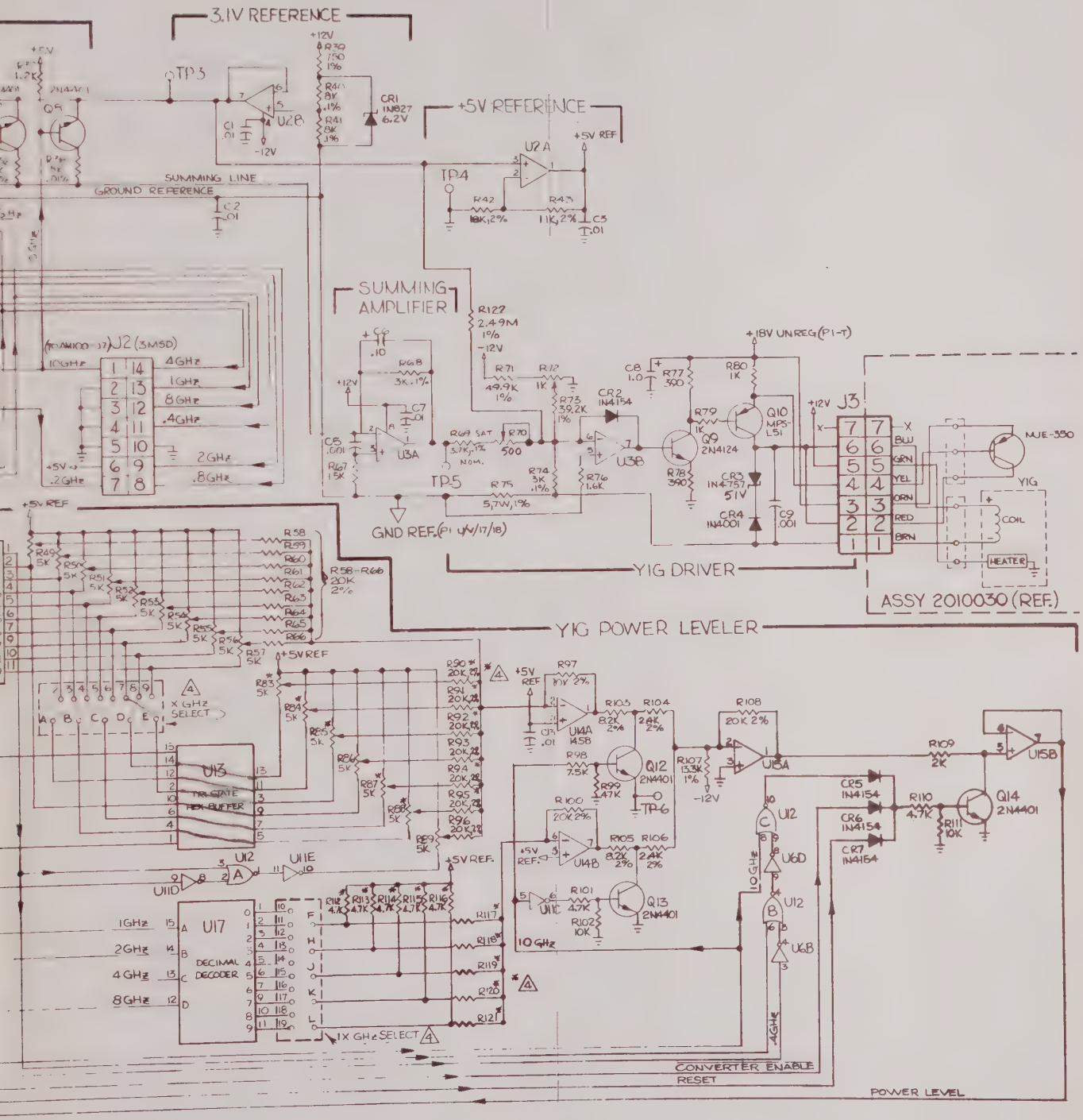
2020067 J

Figure 202a. Component Locator



4 RESISTORS AND POTS INDICATED (*) AND XGHz/YGHz SELECT JUMPERS TO BE INSTALLED AT FINAL TEST A/R. REFER TO TEST PROCEDURE 5540067.

3 J1 USED ONLY WHEN OPTION-01 (PROGRAMMABLE PRESET) OR OPTION-02 (THUMBWHEEL PRESET) ARE USED.



5500067 F

Figure 202b. Schematic Diagram

A203
CONVERTER CONTROL 1

Converter Control 1 performs all the control functions necessary to lock the microwave Converter to the correct YIG/Comb Generator (A207) output frequency, and provide appropriate signals to the direct counter.

Converter Control 1 consists of five basic functional sections: a Video Limiter, a Video Detector, an In-Band Detector, an Analog Processor, and Signal Acquisition Logic. The Video Limiter processes the signal from A204 to provide a constant amplitude signal to the High Frequency board (A106). The Video Detector converts the incoming video signal from A204 to a level proportional to the incoming power. This signal is then compared to a number of preset levels in the Analog Processor circuits, and converted into digital signals for further processing. The In-Band Detector is used to determine whether or not the video frequency falls within the desired passband, and to enable the Analog Processor circuits. The Signal Acquisition Logic provides the digital commands to control the sweep circuits and to lock the Converter on the appropriate comb line.

Figure 203a shows the operating sequence of the Converter. In the absence of an input signal to the Converter, a 200 MHz/ms sweep is continuously generated (DAC 1 ENABLE and CLOCK ENABLE are high). At the end of each sweep, a CONVERTER RESET command is generated (point A to point B on waveform). When a signal is applied, a Video Detector output will be generated when the YIG filter is tuned through the correct harmonic (point C). When this signal appears, a CONVERTER RESET command is again generated (point C to point D), and the sweep is reset to zero. A new sweep is initiated (point D) and eventually the Video Detector again produces an output (point E). At this point, a small backward step will be taken, followed by a 3 millisecond delay (point E to point F). At the end of this time, DAC 2 turns on, and a considerably slower sweep (4 MHz/msec) begins. At point G, the Video Detector output has reached 90% of the value stored in the Peak Detector, and the sweep is stopped. Three milliseconds later (point H), a LOCK command is given, which will allow the counter to read the frequency applied to the High Frequency board (A107). If the sweep is inhibited from stopping at point G (by grounding A203TP4), the Video Detector output will appear as shown by the dotted line on the waveform.

VIDEO LIMITER AND VIDEO DETECTOR

The incoming signal from the Video Amplifier (A204) enters at connector P2, passes through an isolation buffer Q1, and is limited by the differential amplifier Q2-Q4. This provides a fixed output amplitude of approximately 1V peak-to-peak to the High Frequency board. Q1 also drives Video Detector diode CR2. Diode CR3 (matched to CR2) is used for temperature compensation of CR2. The rectified signal is then amplified by U31, whose

gain is set by Video Detector Gain Control R22. The setting of R22 determines the minimum required lock signal from the Video Amplifier. As such, its setting plays an important part in determining the sensitivity of the Converter. Refer to Section 6 for the proper adjustment procedure.

IN-BAND DETECTOR

The Video Amplifier also drives an additional buffer Q6, which provides the drive signal for a two-stage limiter U13. This limiter drives a bandpass filter, whose output is then detected by CR10. (Matched diode CR11 provides temperature compensation for CR10.) The output level of CR10 is thus a function of frequency only. When the output of CR10 exceeds the DC level set by R21, the In-Band Detector triggers, generating a TTL compatible output signal. Trigger level hysteresis prevents the In-Band Detector from turning off until the signal is reduced considerably in power. R64 is set to turn on the In-Band Detector at 250 MHz. Once turned on, it will not turn off until the frequency is increased to approximately 275 MHz. It is this difference in turn-on and turn-off frequency which determines the FM tolerance of the heterodyne Converter at the edge of the video passband.

ANALOG PROCESSOR

The Analog Processor contains a DC-coupled comparator, and a Peak Detector. The purpose of this section is to convert the analog output of the Video Detector into digital commands which can be used to lock the Converter to the correct comb line. U2A compares the Video Detector output to preset levels, and is used to determine that there is sufficient power level from the Video Amplifier. This comparator is enabled by the In-Band Detector output.

Operational amplifiers U3, U4, and associated circuitry, form a Peak Detector which stores the maximum Video Detector output during a particular sweep period. U5A compares the stored output of the Peak Detector with the instantaneous value of the Video Detector output. Switching occurs when that output reaches 90% of the stored peak.

The Peak Detector is discharged by U5B. A CONVERTER RESET command, or lack of the In-Band Detector signal, will activate U5B. The circuit is inhibited from discharging by the presence of the DAC 2 ENABLE command.

The outputs of the two comparators (U2A and U5A), then form input commands to the Signal Acquisition Logic.

SIGNAL ACQUISITION LOGIC

There are five commands generated by the Signal Acquisition Logic: CONVERTER RESET, DAC 1 ENABLE, DAC 2 ENABLE, CLOCK ENABLE, and LOCK. The CONVERTER RESET command is an 18 millisecond pulse used to reset the digital logic on both this board and Converter Control 2 (A202). The three enable commands determine which DAC (if any)

will control the sweep current applied to the YIG filter. If the CLOCK ENABLE is low, no sweep will occur, and the current to the YIG will remain constant. If the CLOCK ENABLE is high, either DAC 1 or DAC 2 (on A202) will generate a current sweep. The appropriate DAC is selected by the DAC ENABLE commands.

The following description is keyed to the corresponding lettered points on the waveforms shown in Figure 203a.

A. Initiation of CONVERTER RESET: A CONVERTER RESET will occur in the digital logic whenever any one of the following occur, (1) CONVERTER RECYCLE command from A104, (2) Either DAC reaching the end of its range, (3) Loss of sufficient video level (U2A input drops below threshold), (4) Image Rejection circuit operating (see later paragraph). When this occurs, U6 pin 1 goes low, causing it to generate an 18 millisecond CONVERTER RESET pulse. This pulse will reset DAC 1, DAC 2, U10B, and U2A.

B. Start Sweep: CONVERTER RESET goes low and enables DAC 1.

C. Presence of Sweep Related Signal: An In-Band signal of sufficient amplitude triggers U2A. When the signal drops below the threshold value, the negative transition triggers flip-flop U10A. This action generates a CONVERTER RESET. All circuits *except* U10A are reset; U10B is enabled.

D. Start of Second Sweep: End of CONVERTER RESET triggers U10B which, in turn, enables U11A. The purpose of the second sweep is to guarantee that after the signal has been applied to the Converter, a sweep is begun from zero frequency. This prevents locking to a harmonic of the input frequency.

E. Presence of Sweep Related Signal: The negative transition of U2A, as described in paragraph C, triggers U11A. This turns on DAC 2 ENABLE. In addition, multivibrator U6A is triggered, which generates a 3 millisecond pulse. The CLOCK ENABLE is turned off during this pulse, and U7A is triggered. The output of U7A enables U7B. The loss of DAC 1 ENABLE also results in a negative current step (generated on Converter Control 2) such that the YIG/Comb Generator is tuned back through the frequency that initiated the trigger. This action causes the twin peaks in the Video Detector output. During this period, the Peak Detector has stored the peak detected signal level; the voltage at U5 pin 6 is 90% of that peak.

F. Start of DAC 2 Sweep: The CLOCK ENABLE command goes high at the end of the pulse from U6A.

G. Stop Sweep: When the Video Detector output reaches 90% of the stored peak, U5A is triggered, which again causes a 3 millisecond pulse to be generated by U6A. This pulse triggers U7B which disables the CLOCK ENABLE.

H. Lock: At the end of the 3 millisecond pulse, the LOCK command is obtained at U9 pin 11 (this allows the counter to display the input frequency). If at any time after LOCK command occurs, the output of the Video Detector should drop below the threshold set at U2 pin 5, a CONVERTER RESET command will be initiated when U2 pin 10 goes high.

IMAGE REJECTION

At input levels below the specified sensitivity, it is possible that although the video level is insufficient to trigger U2A on the correct comb line, the next higher line *is* sufficient. If the counter should lock to this line, called the image, an erroneous reading would result. To prevent this, an image rejection circuit consisting of U11B and U14 is provided.

If the In-Band Detector turns on, then off, without U2A triggering, multivibrator U14B enables flip-flop U11B for 3 milliseconds. If during this period, U2A is triggered, resulting in DAC 1 ENABLE going low, U11B will be triggered, resulting in a CONVERTER RESET. The Converter is thus prevented from locking on the image.

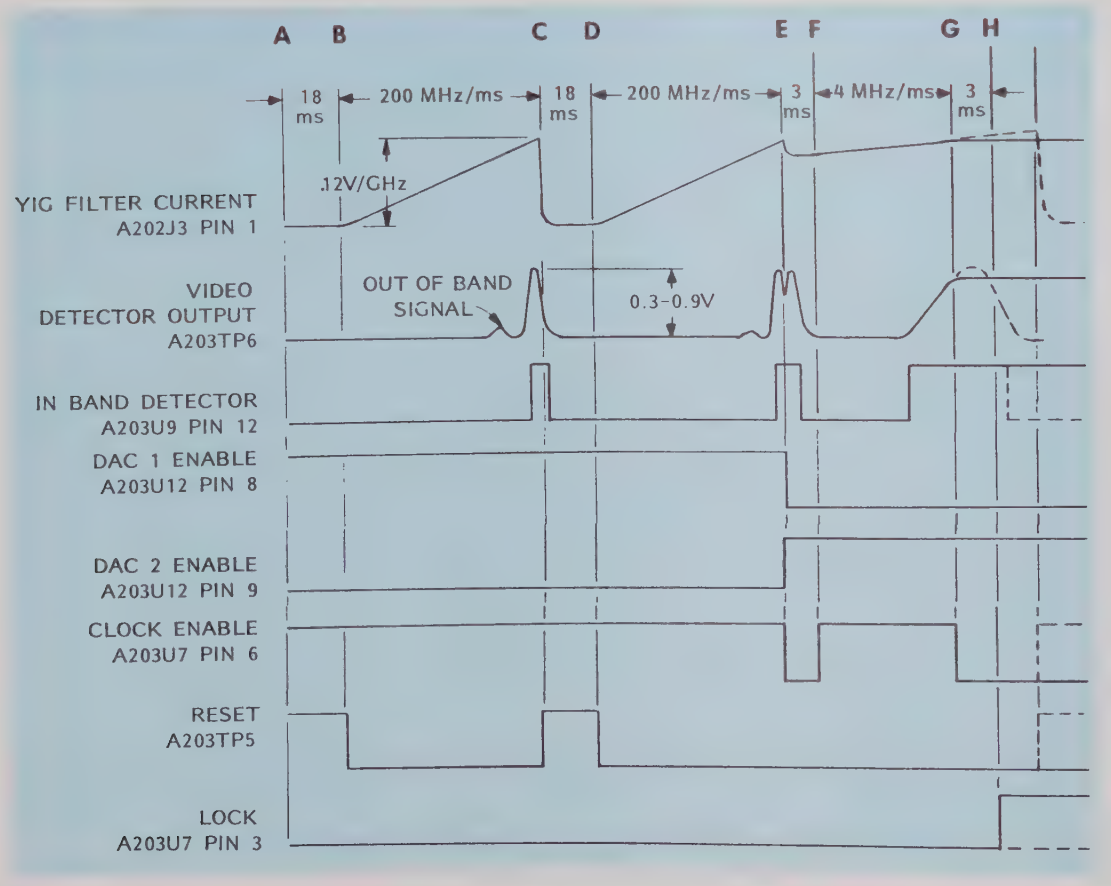


Figure 203a. Operating Sequence Diagram

A203 Converter Control 1

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A203-	Converter Control 1	2020066	1	EIP	
C1	Cer, .001μF, 20%, 1KV	2150001	16	5GA-D10	56289
C2	Cer, 18pF, NPO, 500V	2160007	1	301000C0G0180J	72982
C3 thru C9	C1				
C10	Cer, .01μF, 20%, 100V	2150003	18	TG-S10	56289
C11	C10				
C12	C1				
C13	Cer, .002μF, 20%, 1KV	2150005	1	5GA-D20	56289
C14	Mica, 470pF, 5%, 500V	2250018	1	DM15CD471J0	72136
C15	C10				
C16	Mylar Flm, .039μF, 10%, 100V	2350024	1	225P39391W03	56289
C17	Mica, 56pF, 5%, 500V	2250021	1	DM15CD560J0	72136
C18	C10				
C19	Tant, 1.0μF, 35V	2300008	3	TAG 20-1.0/35-50	14433
C20	C10				
C21	Tant, 4.7μF, 20%, 16V	2300021	1	TAG 20-4.7/16	14433
C22	Tant, 33μF, 20%, 20V	2300023	3	TAG 20-33/20	14433
C23	C10				
C24 thru C28	C1				
C29	Mica, 180pF, 5%, 500V	2250006	2	DM15CD181J0	72136
C30	C29				
C31	Cer, 15pF, NPO, 500V	2160006	1	301000C0G0150J	72982
C32	Cer, 4.7pF, NPO, 500V	2160013	1	301000C0H0479J	72982
C33	C31				
C34	C31				
C35	C10				
C36	C10				
C37	Mica, 680pF, 5%, 500V	2250026	1	DM15CD581J0	72136
C38	Cer, .05μF, 20%, 100V	2150009	1	TG-S50	56289
C39	Tant, .15μF, 35	2300003	1	TAG 20-0.15/35-50	14433
C40	C19				
C41	Mica, 68pF, 5%, 500V	2250025	1	DM15CD680J0	72136
C42	C19				
C43	C10				
C44	C10				
C45	Tant, 10μF, 25V	2300029	2	TAG 20-10/25	14433
C46	C10				
C47	C22				

A203 Converter Control 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C48	C10				
C49	C10				
C50	C22				
C51	C10				
C52	C10				
C53	C45				
C54 thru C56	C10				
C57	Mica, 7pF, 10%, 500V	2250031	1	DM15CD7R0K0	72136
CR1	Gen. Purp.	2704151	3	1N4154	07263
CR2	Hot Carr	2710014	2	FH1100	EIP
CR3	C2				
CR4	CR1				
CR5	Lo-Lkge	2710013	1	DX100	32293
CR6	Zen, 5.1V	2705231	1	1N5231	04713
CR7	Zen, 3.6V	2705227	1	1N5227	04713
CR8	Zen, 8.2V	2705237	1	1N5237	04713
CR9	CR1				
CR10	CR2				
CR11	CR2				
L1	Ind: 1.0μH	3510003	1	DD-1.00	72259
L2	Part of PC Board				
L3	Ind: 0.1μH	3510001	2	DD-0.10	72259
L4	Part of PC Board				
L5	Part of PC Board				
L6	Ind: 0.33μH	3510007	1	1025-08	99800
L7	Part of PC Board				
L8	Part of PC Board				
L9	L3				
Q1	Sel, 2N5179, YEL	4710012	3	4705179, EIP	
Q2	PNP, RF	4710010	1	MPS-H81	04713
Q3	NPN, RF SW	4710017	1	MMT-3960	04713
Q4	Q1				
Q5	NPN, GP	4704124	1	2N4124	04713
Q6	Q1				
R1	Comp, 150 ohms, 5%	4010151	1	RC07GF151J	81349
R2	Comp, 2.7K, 5%	4010272	1	RC07GF272J	81349
R3	Comp, 100 ohms, 5%	4010101	3	RC07GF101J	81349

A203 Converter Channel 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R4	Comp, 510 ohms, 5%	4010511	2	RC07GF511J	81349
R5	Comp, 27 ohms, 5%	4010270	2	RC07GF270J	81349
R6	Comp, 2.2K, 5%	4010222	4	RC07GF222J	81349
R7	Comp, 33 ohms, 5%	4010330	2	RC07GF330J	81349
R8	Comp, 1K, 5%	4010102	8	RC07GF102J	81349
R9	R7				
R10	Comp, 220 ohms, 5%	4010221	1	RC07GF221J	81349
R11	Comp, 270 ohms, 5%	4010271	2	RC07GF271J	81349
R12	R8				
R13	Comp, 330 ohms, 5%	4010331	3	RC07GF331J	81349
R14	Comp, 75 ohms, 5%	4010750	2	RC07GF750J	81349
R15	Comp, 180K ohms, 5%	4010184	4	RC07GF184J	81349
R16	Met Ox, 10K, 2%	4130103	2	C4/2%/10K	24546
R17	R16				
R18	R15				
R19	R14				
R20	Comp, 3.3K, 5%	4010332	1	RC07GF332J	81349
R21	Comp, 6.2K, 5%	4010622	1	RC07GF622J	81349
R22	Var, Cer, 10K	4250006	1	72XWR10K	73138
R23	R8				
R24	Comp, 11K, 5%	4010113	2	RC07GF113J	81349
R25	R11				
R26	Comp, 36K, 5%	4010363	1	RC07GF363J	81349
R27	Comp, 4.7K, 5%	4010472	3	RC07GF472J	81349
R28	Comp, 10K, 5%	4010103	6	RC07GF103J	81349
R29	R8				
R30	Comp, 300 ohms, 5%	4010301	1	RC07GF301J	81349
R31	Comp, 200 ohms, 5%	4010201	2	RC07GF201J	81349
R32	Comp, S.A.T.	4010999	1	(200 ohms nom.)	81349
R33	Comp, 1.8K, 5%	4010182	1	RC07GF182J	81349
R34	R27				
R35	Comp, 68K, 5%	4010683	1	RC07GF683J	81349
R36	R28				
R37	Comp, 1.5K, 5%	4010152	1	RC07GF152J	81349
R38	R8				
R39	Comp, 12K, 5%	4010123	2	RC07GF123J	81349
R40	Comp, 2K, 5%	4010202	1	RC07GF202J	81349
R41	R28				
R42	R27				
R43	R24				
R44	R28				
R45	R28				
R46	R4				

A203 Converter Channel 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R47	Comp, S.A.T.	4010999	1	(100 ohms nom.)	81349
R48	R31				
R49	R5				
R50	R8				
R51	R6				
R52	R6				
R53	Comp, 51 ohms, 5%	4010510	3	RC07GF510J	81349
R54	Comp, 130 ohms, 5%	4010131	1	RC07GF131J	81349
R55	R53				
R56	R13				
R57	R8				
R58	R6				
R59	Comp, 750 ohms, 5%	4010751	1	RC07GF751J	81349
R60	Comp, 110 ohms, 5%	4010111	2	RC07GF111J	81349
R61	R60				
R62	R13				
R63	R53				
R64	Var, 100 ohms	4250001	1	72XWR100	73138
R65	R15				
R66	R15				
R67	Comp, 9.1K, 5%	4010912	1	RC07GF912J	81349
R68	Comp, 8.2K, 5%	4010822	2	RC07GF822J	81349
R69	Comp, S.A.T.	4010999	1	(8.2K nom.)	81349
R70	Comp, 30K, 5%	4010303	1	RC07GF303J	81349
R71	R8				
R72	R28				
R73	R68				
R74	Prec, 7.15K, 1%	4057151	2	RN55C7151F	81349
R75	R74				
R76	R39				
R77	Comp, 13K, 5%	4010133	1	RC07GF133J	81349
R78	R3				
R79	R3				
R80	Met Ox, 15K, 2%	4130153	1	C4/2%/15K	24546
TP1 thru TP8	Conn, PC Pin, Gold	2620032	8	460-2970-02-03	71279
U1	Op Ampl, Hi Slew RT	3041741	1	MC1741SCP1	0000X
U2	Dual Comparator	3072506	2	SN72506N	0000X
U3	Op Ampl	3040741	1	LM741CN	0000X
U4	Op Ampl, COS/MOS	3043130	1	CA3130E	0000X

A203 Converter Channel 1 (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
U5	U2				
U6	TTL, Monostable MV	3074123	2	DM74123	0000X
U7	Dual J-K Flip-flop	3087473	3	DM74LS73	0000X
U8	Quad, 21NP, NAND Gate	3087400	1	DM74LS00	0000X
U9	Quad, 21NP, AND Gate	3087408	1	SN7408N	0000X
U10	U7				
U11	U7				
U12	Hex Inverter	3087405	1	DM74LS05	0000X
U13	Dual, Diff. Ampl	3043049	1	CA3049T	0000X
U14	TTL, Monostable MV	3087423	1	DM74LS123	0000X
U15	8-Bit, D/A Converter	3011408	1	MC1408L6	0000X
U16	Dual, 4-Bit, BIN Counter	3084393	1	DM74LS393	0000X
U17	Dual, 41NP, NAND Gate	3087420	1	DM74LS20	0000X
U18	U6				

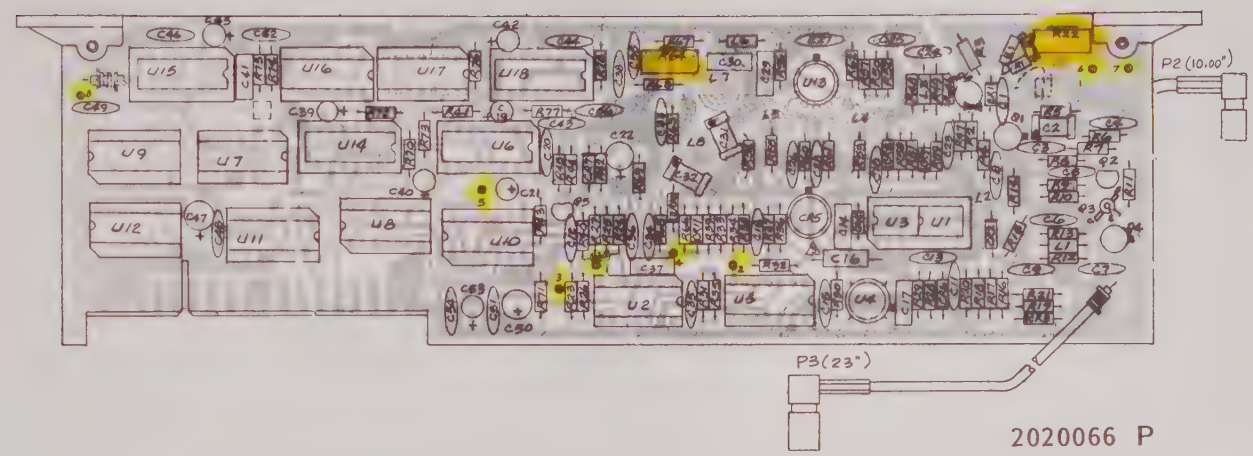
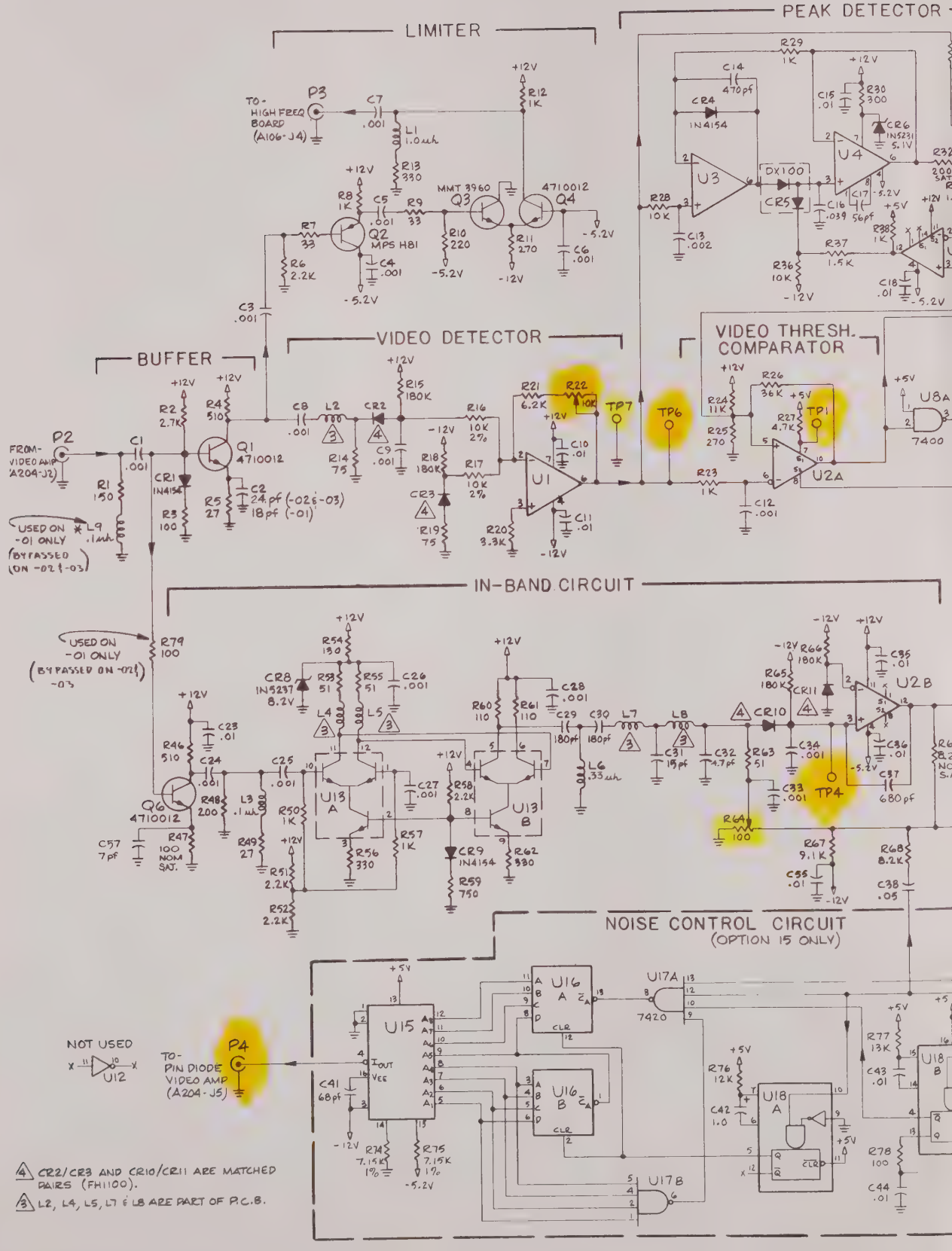
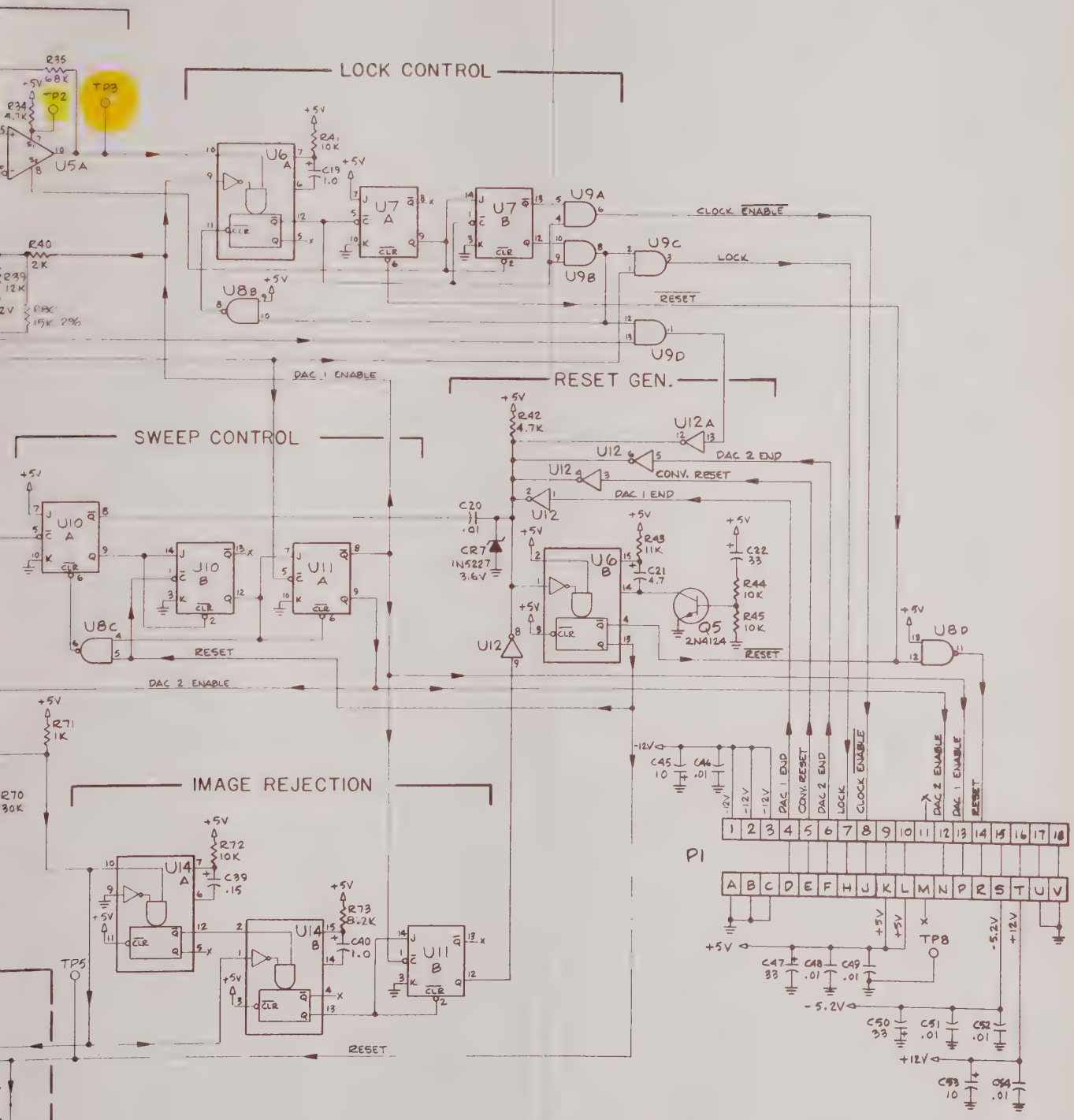


Figure 203b. Component Locator


LIMITER
PEAK DETECTOR
BUFFER
VIDEO DETECTOR
VIDEO THRESH. COMPARATOR
IN-BAND CIRCUIT
NOISE CONTROL CIRCUIT
(OPTION 15 ONLY)
TO- HIGH FREQ BOARD (A106-J4)
FROM- VIDEO AMP (A204-J2)
USED ON -01 ONLY
(BYPASSED ON -02 & -03)
USED ON -01 ONLY
(BYPASSED ON -02 & -03)
TO- PIN DIODE VIDEO AMP (A204-J5)
NOT USED
MMT 3960
MPS H81
DX100
7400
7420
TP1
TP4
TP6
TP7
4 CR2/CR3 AND CR10/CR11 ARE MATCHED PAIRS (FH1100).
3 L2, L4, L5, L7 & L8 ARE PART OF P.C.B.



5500066-03 G

Figure 203c. Schematic Diagram

A204
VIDEO AMPLIFIER

The difference frequency generated in the Mixer (A205) is applied to the input connector J1 of the Video Amplifier. The amplified output at J2 is sent to Converter Control 1 (A203) for further processing.

The circuitry consists of six essentially identical gain blocks and an automatic gain control circuit. Overall gain of the unit is nominally 56 dB with a frequency range of 25 MHz to 275 MHz. A block diagram of A204 is shown in Figure 204a.

Each gain block includes a broadband feedback pair Q1-Q2, an emitter follower Q3, band shaping C4-C5, and bias circuitry. Overall gain per block is approximately 10 dB.

The normal gain control circuit consists of a level detector composed of CR23 and CR24, the loop amplifier U4, PIN current driver Q20, and PIN attenuator diodes CR3, CR6, and CR11.

Once this loop has turned on, a memory circuit serves to hold the gain reduced for a period of time. This is to assist in the centering of the YIG Filter passband on a comb line as discussed under Converter Control 1 (A203). This circuit consists of the peak detector formed by U2, U3, and associated elements. Gate diodes CR18 and CR19 give control of the agc system to the lowest of the outputs of U2 or U4.

The remaining circuitry on A204 reduces the maximum available gain at high RF power levels (greater than -10 dBm). The DC output current (negative) from the Mixer is a measure of RF input power. As this current increases, the output from U1 increases from its initial value of -7.5 volts towards 0 volts. This varies the level at which Q21 turns on, which, in turn, sets the maximum output of U4. Q19 forms a clamp so that there is a limit to how far the gain may be reduced.

A204 Video Amplifier

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A204	Video Amplifier	2020014	1	EIP	
C1	Cer, .01μF, 20%, 50V	2150003	27	TG-S10	95275
C2	Modified 2150003	5280013	1	EIP	
C3	C1				
C4	Cer, S.A.T.	2160999	10	1.0pF Nom.	72982
C5	C4				
C6	Cer, .001μF, 20%, 1 KV	2150001	13	5GA-D10	56289
C7	C1				
C8	C6				
C9	C6				
C10	C1				
C11	C4				
C12	C1				
C13	C1				
C14	C6				
C15	C6				
C16	C1				
C17	C4				
C18	C6				
C19	C1				
C20	C1				
C21	C6				
C22	C1				
C23	C4				
C24	C6				
C25	C1				
C26	C6				
C27	C1				
C28	C4				
C29	C1				
C30	C6				
C31	C6				
C32	C1				
C33	Cer, 2.2pF, NPO, 500V	2160008	1	301000C0J0229C	72982
C34	C4 (10pF nom.)				
C35	Mica, 300pF, 5%, 500V	2250013	2	DM15CD301JO	72136
C36	C35				
C37	C1				
C38	C1				
C39	Tant, 10μF, 25V	2300029	2	TAG 20-10/25	14433
C40	Ref. (on assy. 2010010)				
C41	Mica, 200pF, 5%, 500V	2250009	1	DM15CD201JO	72136

A204 Video Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C42 thru C44	C1				
C45	Not Used				
C46	Cer, .002μF, 20%, 1KV	2150005	3	5GA-D20	56289
C47	C46				
C48	C6				
C49	C1				
C50	C1				
C51	Tant, 1μF, 35V	2300008	1	TAG 20-1.0/35	14433
C52	C6				
C53	C1				
C54	C1				
C55	C46				
C56	C1				
C57	C1				
C58	C4				
C59	Mica, 470pF, 5%, 500V	2250018	1	DM15CD471JO	72136
C60	C39				
C61	C1				
C62	Ref. (on assy. 2010010)				
C63	Not Used				
C64	C4				
C65	C4				
C66	C1				
CR1	G.P.	2704154	19	1N4154	07263
CR2	CR1				
CR3	Pin	2710024	2	MA47123	96341
CR4	CR1				
CR5	CR1				
CR6	Pin	2710022	1	MA47110	96341
CR7 thru CR10	CR1				
CR11	CR3				
CR12 thru CR16	CR1				
CR17	Not Used				
CR18 thru CR22	CR1				

A204 Video Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
CR23	Hot Carr	2710004	2	FH1100	07263
CR24	CR23				
CR25	CR1				
L1	Ind, 0.1μH	3510001	1	DD-0.10	72259
L2	Ind, .68μH	3510009	1	DD-0.68	72259
L3	Ind, 2.2μH	3510005	1	DD-2.20	72259
Q1	Sel, 2N5179 - GRN	4710013	6	4705179	EIP
Q2	PNP, RF	4710010	8	MPS-H81	04713
Q3	Sel, 2N5179 - YEL.	4170012	4	4705179	EIP
Q4	Q1				
Q5	Q2				
Q6	Q3				
Q7	Q1				
Q8	Q2				
Q9	Q3				
Q10	Q1				
Q11	Q2				
Q12	Q3				
Q13	Q1				
Q14	Q2				
Q15	Q2				
Q16	Q1				
Q17	Q2				
Q18	Q2				
Q19	NPN, G.P.	4704124	4	2N4124	04713
Q20	Graded, 2N5179 - RED	4710011	1	EIP	
Q21 thru Q23	Q19				
R1	Comp, 150 ohms, 5%	4010151	1	RC07GF151J	81349
R2	Comp, 4.3K ohms, 5%	4010432	6	RC07GF432J	81349
R3	Comp, 560 ohms, 5%	4010561	6	RC07GF561J	81349
R4	Comp, 270 ohms, 5%	4010271	7	RC07GF271J	81349
R5	Comp, 39 ohms, 5%	4010390	9	RC07GF390J	81349
R6	Comp, 18 ohms, 5%	4010180	6	RC07GF180J	81349
R7	Comp, 100 ohms, 5%	4010101	6	RC07GF101J	81349
R8	Comp, 36 ohms, 5%	4010360	6	RC07GF360J	81349
R9	Comp, 510 ohms, 5%	4010511	5	RC07GF511J	81349
R10	R5				
R11	R7				

A204 Video Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R12	R2				
R13	R3				
R14	R4				
R15	R5				
R16	R6				
R17	R7				
R18	R8				
R19	R9				
R20	R5				
R21	Comp, 51 ohms, 5%	4010510	4	RC07GF510J	81349
R22	R2				
R23	R3				
R24	R4				
R25	Comp, 47 ohms, 5%	4010470	1	RC07GF470J	81349
R26	R5				
R27	R6				
R28	R7				
R29	R8				
R30	R9				
R31	R21				
R32	R2				
R33	R3				
R34	R4				
R35	R5				
R36	R6				
R37	R7				
R38	R8				
R39	R9				
R40	R5				
R41	R21				
R42	R2				
R43	R3				
R44	R4				
R45	R5				
R46	R6				
R47	Comp, 82 ohms, Nom., S.A.T., 5%	4010820	1	RC07GF820J	81349
R48	R8				
R49	Comp, 1.2K ohms, 5%	4010122	3	RC07GF122J	81349
R50	Comp, 75 ohms, 5%	4010750	1	RC07GF750J	81349
R51	R2				
R52	R3				
R53	R4				
R54	R5				

A204 Video Amplifier (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R55	R6				
R56	R7				
R57	R8				
R58	R49				
R59	Comp, 24K ohms, 5%	4010243	1	RC07GF243J	81349
R60	Comp, 15K ohms, 5%	4010153	1	RC07GF153J	81349
R61	R49				
R62	Comp, 47K ohms, 5%	4010473	2	RC07GF473J	81349
R63	Comp, 9.1K ohms, 5%	4010912	1	RC07GF912J	81349
R64	Comp, 2.7K ohms, 5%	4010272	1	RC07GF272J	81349
R65	Comp, 180 ohms, 5%	4010181	3	RC07GF181J	81349
R66	Not Used				
R67	Not Used				
R68	R65				
R69	Not Used				
R70	R65				
R71	Comp, 2.2K ohms, 5%	4010222	2	RC07GF222J	81349
R72	Comp, 22M ohms, 5%	4010226	1	RC07GF226J	81349
R73	Comp, 1K, 5%	4010102	1	RC07GF102J	81349
R74	Not Used				
R75	Comp, 10K, 5%	4010103	2	RC07GF103J	81349
R76	Comp, 1.3K, 5%	4010132	1	RC07GF132J	81349
R77	Comp, 11K, 5%	4010113	1	RC07GF113J	81349
R78	Comp, 2.4K, 5%	4010242	1	RC07GF242J	81349
R79	Comp, 4.7K, 5%	4010472	1	RC07GF472J	81349
R80	R9				
R81	R4				
R82	Comp, 6.2K, 5%	4010622	1	RC07GF622J	81349
R83	Comp, 27 ohms, 5%	4010270	1	RC07GF270J	81349
R84	Comp, 200 ohms, 5%	4010201	1	RC07GF201J	81349
R85	Comp, 1.5K, 5%	4010152	1	RC07GF152J	81349
R86	R21				
R87	R71				
R88	R75				
R89	Comp, 6.8K, 5%	4010682	1	RC07GF682J	81349
R90	R62				
U1 thru U4	Op Amplifier	3040741	4	LM741CN	

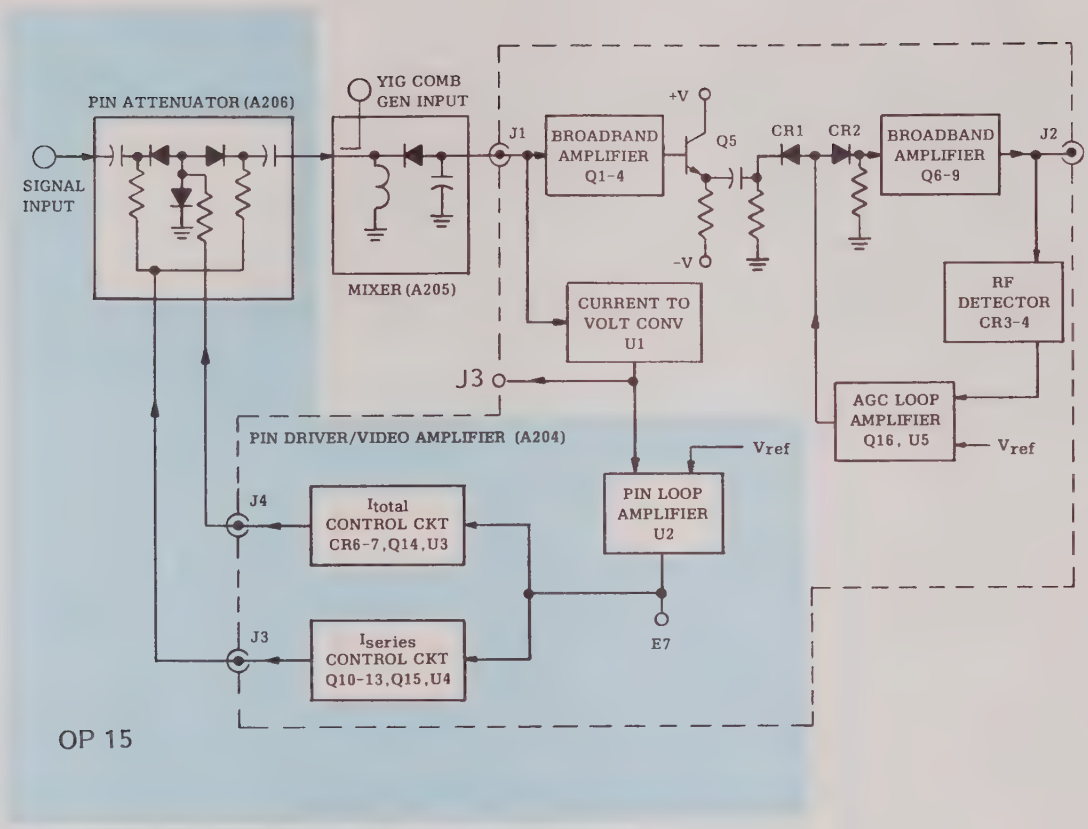


Figure 204a. Video Amplifier Diagram

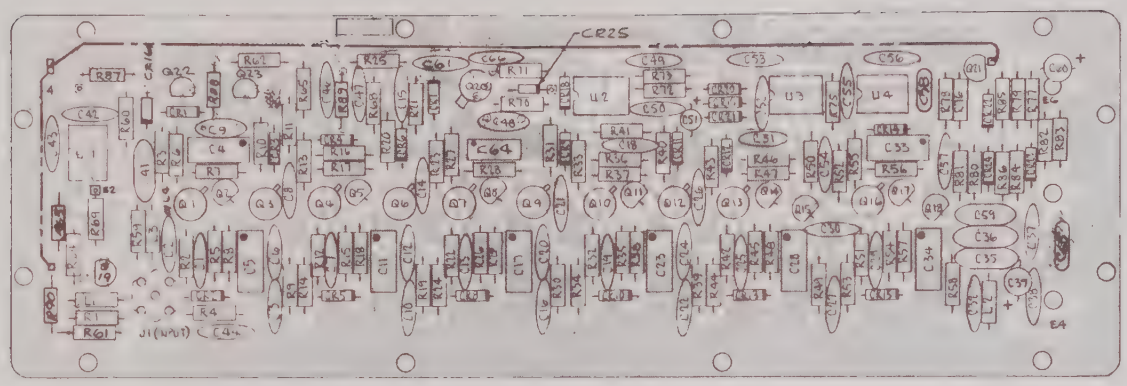


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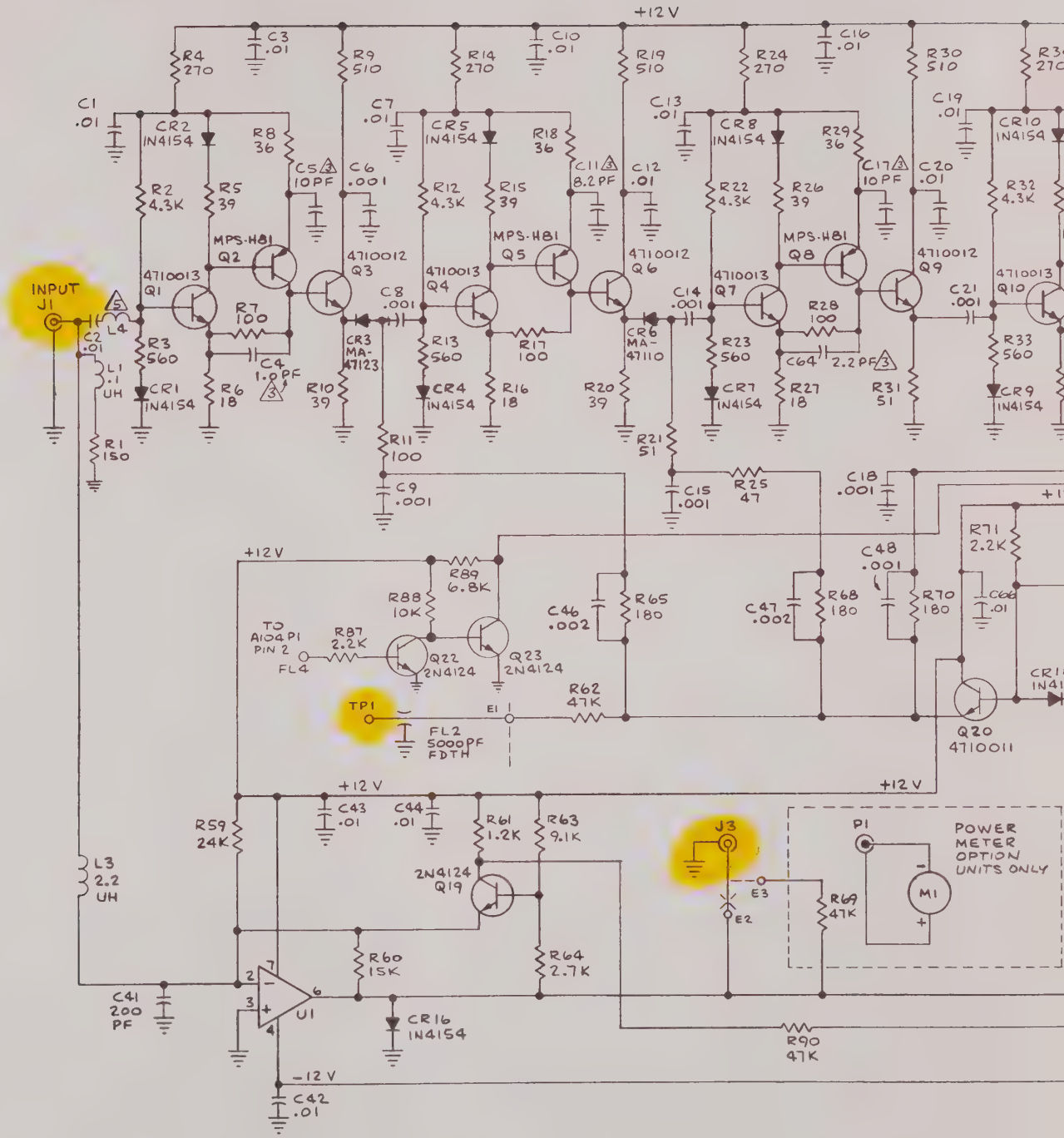
Figure 204b. Component Locator


+12 V
INPUT
J1
C1 .01
C2 .01
L4
L1 .1 UH
R1 150
R2 4.3K
R3 560
R4 270
R5 39
R6 18
R7 100
R8 36
R9 510
R10 39
R11 100
R12 4.3K
R13 560
R14 270
R15 39
R16 18
R17 100
R18 36
R19 510
R20 39
R21 51
R22 4.3K
R23 560
R24 270
R25 47
R26 39
R27 18
R28 100
R29 36
R30 510
R31 51
R32 4.3K
R33 560
C3 .01
C4 1.0 PF
C5 10PF
C6 .001
C7 .01
C8 .001
C9 .001
C10 .01
C11 8.2 PF
C12 .01
C13 .01
C14 .001
C15 .001
C16 .01
C17 10PF
C18 .001
C19 .01
C20 .01
C21 .001
C64 2.2 PF
CR1 IN4154
CR2 IN4154
CR3 MA-47123
CR4 IN4154
CR5 IN4154
CR6 MA-47110
CR7 IN4154
CR8 IN4154
CR9 IN4154
CR10 IN4154
Q1 4710013
Q2 MPS-H81
Q3 4710012
Q4 4710013
Q5 MPS-H81
Q6 4710012
Q7 4710013
Q8 MPS-H81
Q9 4710012
Q10 4710013
R71 2.2K
C48 .001
R89 6.8K
R88 10K
R87 2.2K
TO A104 P1 PIN 2
FL4
Q22 2N4124
Q23 2N4124
C46 .002
R65 180
C47 .002
R68 180
R70 180
TP1
E1
FL2 5000PF FDTH
R62 47K
Q20 4710011
+12 V
C43 .01
C44 .01
R59 24K
R61 1.2K
R63 9.1K
L3 2.2 UH
2N4124 Q19
J3
E3
E2
P1
POWER METER OPTION UNITS ONLY
M1
R69 47K
R60 15K
R64 2.7K
C41 200 PF
U1
CR16 IN4154
R90 47K
-12 V
C42 .01

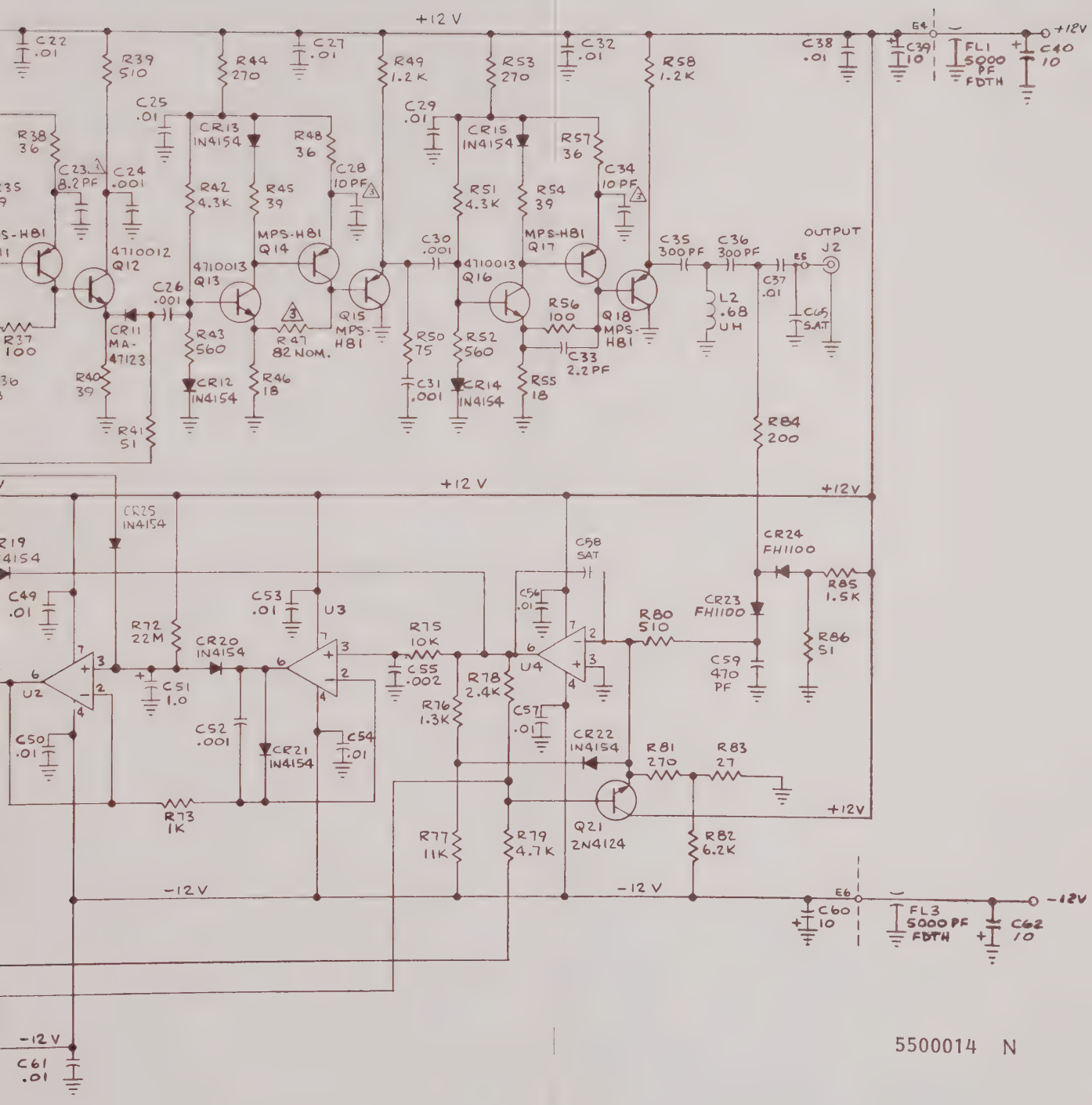
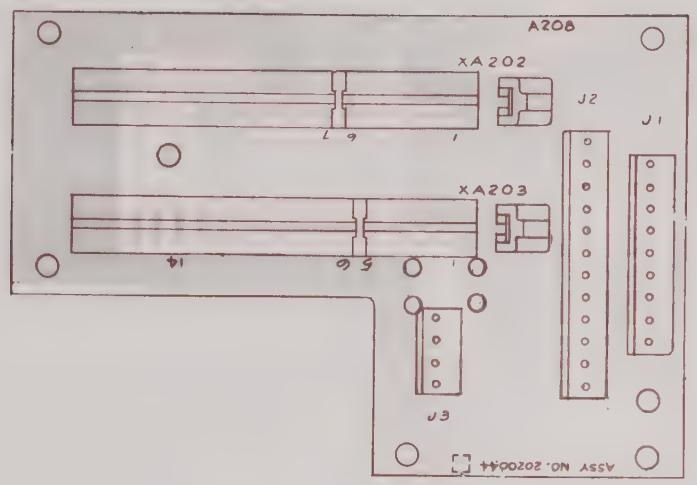


Figure 204c. Schematic Diagram

A208
CONVERTER INTERCONNECTION

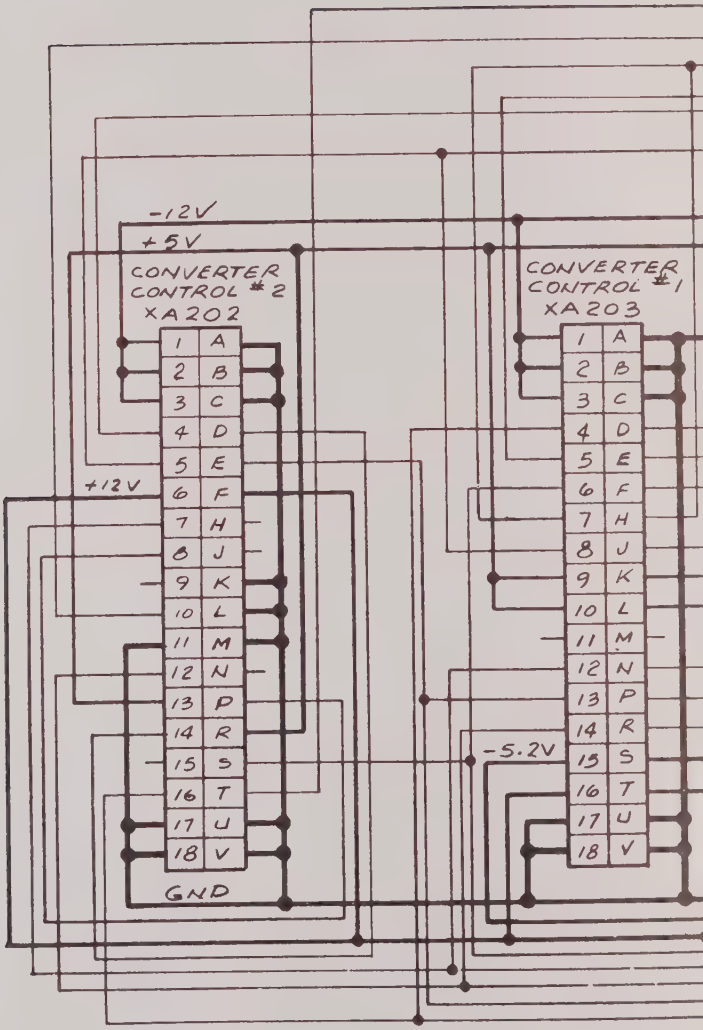
The Converter Interconnection Board (A208) contains the interconnection wiring for the converter section as well as the interface connection between the Counter and Converter. Power to all converter assemblies is distributed by this board.

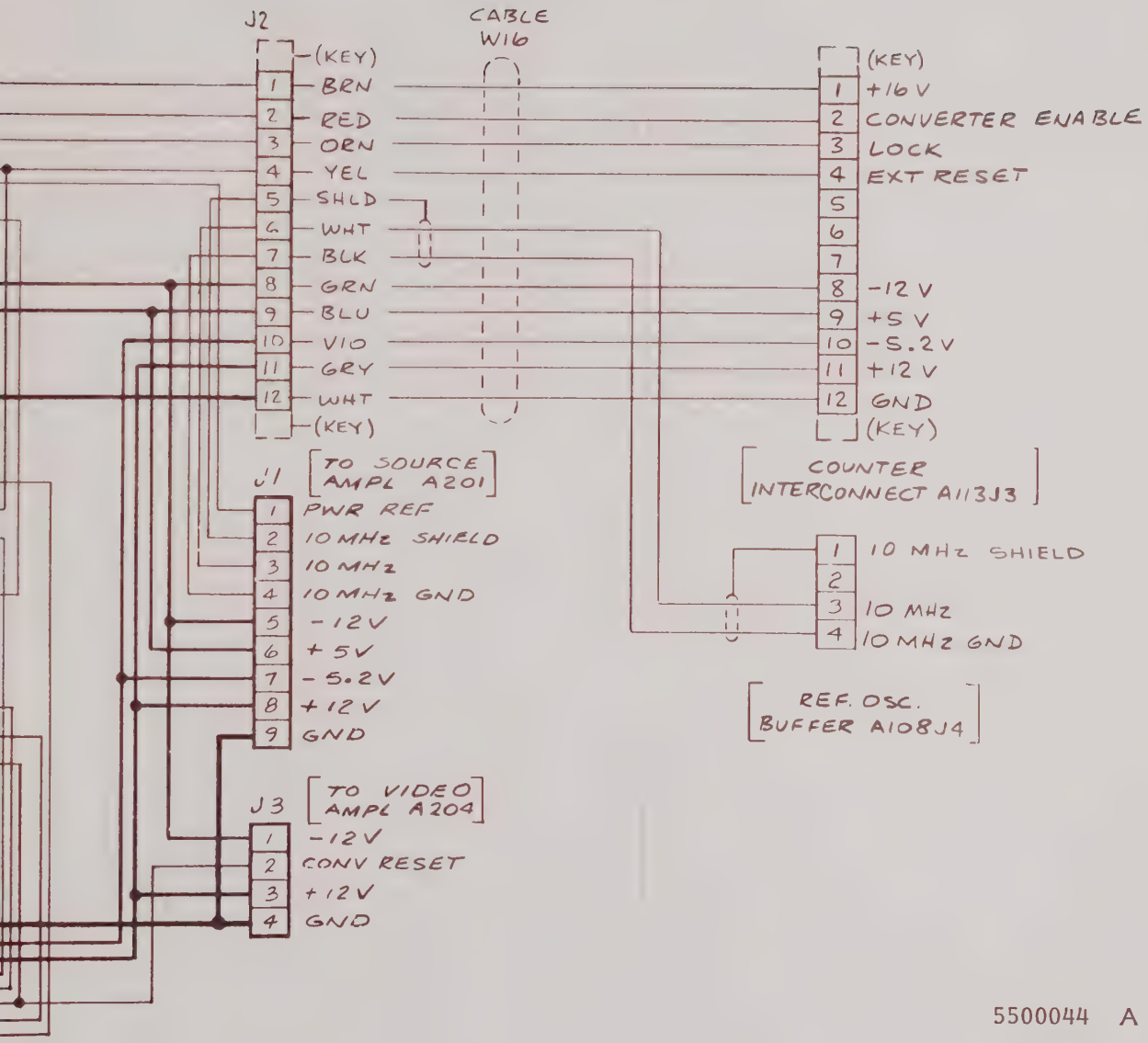


2020044 A

Figure 208a. Component Locator

5580007


-12V
+5V
CONVERTER CONTROL #2
XA202
+12V
GND
CONVERTER CONTROL #1
XA203
-5.2V
1 A
2 B
3 C
4 D
5 E
6 F
7 H
8 J
9 K
10 L
11 M
12 N
13 P
14 R
15 S
16 T
17 U
18 V



5500044 A

Figure 208b. Schematic Diagram

Appendix A
List of Manufacturers

FSCM	MFR NAME, ADDRESS, ZIP CODE
01121	Allen-Bradley Co., So. Milwaukee, WI 53204
01295	Texas Instruments, Inc., Dallas, TX 75222
02600	Amphenol Connector Div., Bunker Ramo Corp., Broadview, IL 60153
04618	American Pancor, Inc., Paoli, PA 19301
04713	Semiconductor Div., Motorola, Inc., Phoenix, AZ 85008
05591	General Resistance Div., Chronetics, Inc., Mt. Vernon, NY 10550
06665	Precision Monolithics, Santa Clara, CA 95050
07263	Fairchild Semiconductor, Mountain View, CA 94040
09353	C and K Components, Inc., Watertown, MA 02172
11236	CTS of Berne, Inc., Berne, IN 46711
11532	Teledyne Relays, Hawthorne, CA 90250
12436	General Dynamics Corp., San Diego, CA 92112
14099	Semtech Corp., Newbury Park, CA 91320
14298	American Components, Inc., Conshohocken, PA 19428
14433	ITT Semiconductor Div. of ITT Corp., W. Palm Beach, FL 33401
20754	KMC Semiconductor Corp., Long Valley, NJ 07853
21793	Dana Laboratories Inc., Irvine, CA 92664
23880	Stanford Applied Engineering, Inc., Santa Clara, CA 95050
23936	Pamotor, Inc., Burlingame, CA 94010
26654	Varadyne Industries, Santa Monica, CA 90404
28480	Hewlett-Packard Co., Palo Alto, CA 94304
32293	Intersil Inc., Cupertino, CA 95014
34649	INTEL Corp., Santa Clara, CA 95051
50522	Electronic Special Products, Monsanto Co., Cupertino, CA 95014
50579	Litronix, Inc., Cupertino, CA 95014
56289	Sprague Electric Co., North Adams, MA 01247
70903	Belden Corp., Chicago, IL 60644
71279	Cambridge Thermionic Corp., Cambridge, MA 02138
71400	Bussman Mfg. Div., McGraw-Edison Co., St. Louis, MO 63107
71590	Centralab Div., Globe-Union, Inc., Milwaukee, WI 53201
71785	Cinch Div., TRW Electronic Components, Elk Grove Village, IL 60007
72136	Electro-Motive Mfg. Co., Willimantic, CT 06226
72259	Nytronics, Inc., Pelham Manor, NY 10803
72982	Erie Technological Products, Inc., Erie, PA 16512
73138	Helipot Div., Beckman Instruments, Fullerton, CA 92634
75915	Littelfuse, Inc., Des Plaines, IL 60016
76854	Oak Mfg. Div., Oak Electro/Netics Corp., Crystal Lake, IL 60014
80031	Mepco/Electra, Inc., Morristown, NJ 07960
80294	Instrument Div., Bourns, Inc., Riverside, CA 92506
81349	Military Specification
82389	Switchcraft, Inc., Chicago, IL 60630
86797	Rogan Bros., Inc., Skokie, IL 60076
88140	Cutler-Hammer, Inc., Lincoln, IL 62656
91637	Kings Electronics Co., Tuckahoe, NY 10707
95275	Vitramon, Inc., Bridgeport, CT 06601
96341	Microwave Associates, Burlington, MA 01801
98291	Sealectro, Mamaroneck, NY 10544
99800	Delavan Div., American Precision Indust., East Aurora, NY 14052
	FOLLOWING MFRS DO NOT HAVE FSCM NUMBER
0000A	Molex, Inc., Lisle, IL 60532
0000B	Stettner-Thrush, Cazenovia, NY 13035
0000C	Plessey Electric-Products, Los Angeles, CA 90066
0000L	Rohm Corporation, Irvine, CA 92664
0000S	California Eastern Labs., Burlingame, CA 94010
0000T	Data Display Products, Los Angeles, CA 90009
0000X	Any Manufacturer of This Product

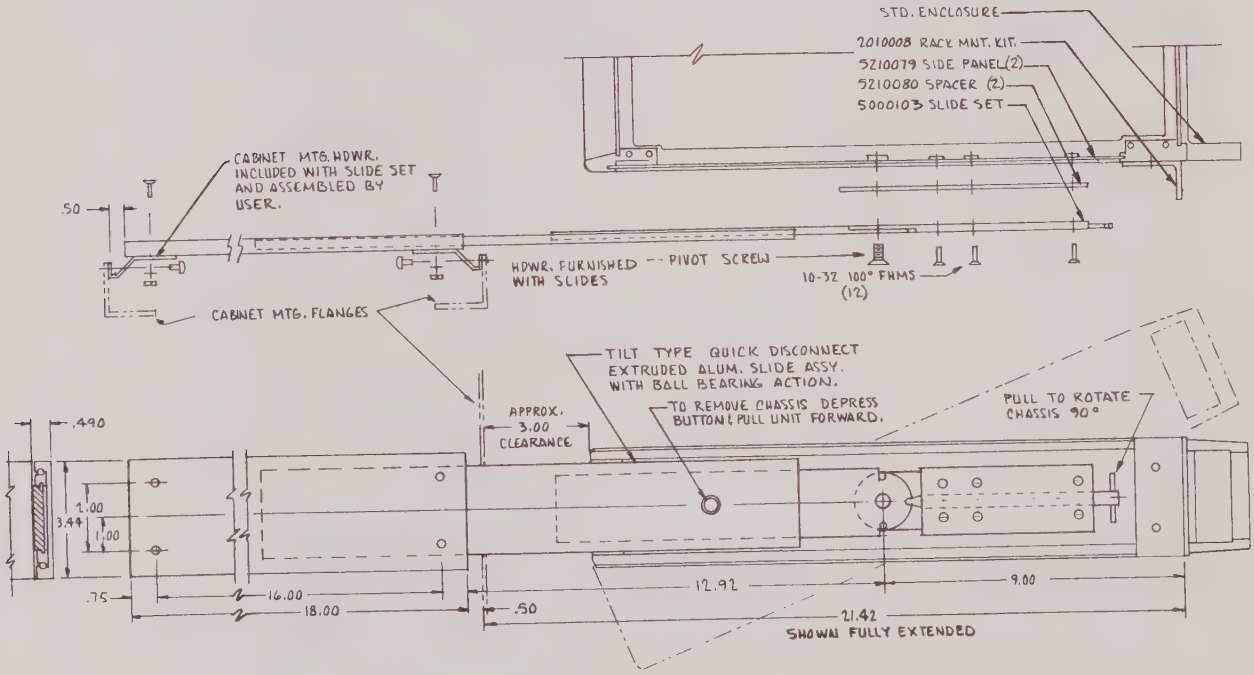
Appendix B
Options

Appendix B provides descriptions, specifications (where applicable), schematic diagrams and component locators for the options available for use with the Model 331 Counter.

Option	
13	Rack Mount/Chassis Slide
15	Automatic Input Level Control
16	General Purpose Interface Buss (See separate manual)
31	Programming
32	YIG Preset, Thumbwheel
36	Programming Offsets
39	BCD Output

13-1. GENERAL

To install slides in field, remove top cover and top frame of counter. Mount the special side panels (P/N 5210079) in place of the standard side panels. Replace top frame and top cover of counter.



NOTES:

1. ALL MOUNTING HARDWARE AND HOLE SPACING CONFORMS TO MIL-STD-189.

Figure 13-1. Installation Diagram

OPTION 15
AUTOMATIC INPUT LEVEL CONTROL

15-1. GENERAL

Option 15 provides a closed loop leveling system at the input to the counter which maintains a relatively constant input level to the Mixer (approximately -20 dBm). This results in an improvement in the burnout level (+30 dBm compared to +20 dBm of a standard unit), and an increase in the operating signal level. Typically, operation up to +20 dBm is possible and sensitivity is increased by 5 dBm over the entire operating range of the counter. In addition, Option 15 provides improved measurement capability in the presence of spurious signals and wideband noise. Refer to Table 15-1 for specifications pertinent to this option.

Table 15-1. Specifications

Maximum input level (burnout):	+30 dBm (1 W)
Maximum operating level (typ):	+20 dBm (100 mW)
Dynamic operating range (typ):	Approximately 45 dB
Sensitivity:	
.825 - 1.1 GHz:	- 20 dBm
1.1 - 12.4 GHz :	-25 dBm
12.4 - 18 GHz :	-20 dBm

15-2. OPERATION

A functional block diagram of the Automatic Level Control System is shown in Figure 15-1. Input RF power is detected in the Mixer (A205), producing a current proportional to the input power. When this current exceeds a value determined by the threshold circuit, the PIN driver is turned on, thus increasing the insertion loss through the PIN Diode Attenuator (A206).

The PIN Diode Attenuator contains series and shunt diodes, arranged in such a manner that when appropriate currents are applied, insertion loss can be varied while both input and output ports maintain a nominal 50Ω impedance. The PIN Driver contains appropriate shaping networks to supply the correct currents at all attenuation levels.

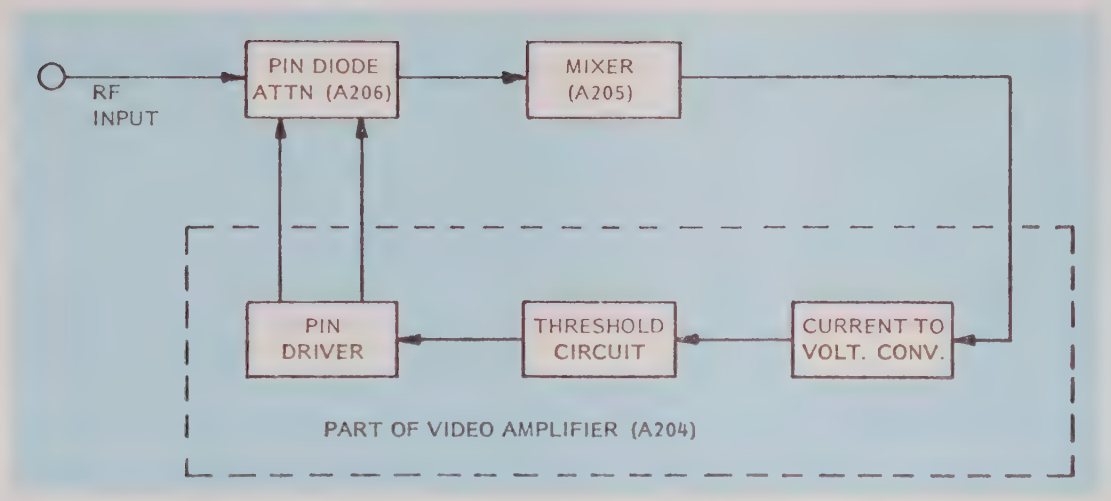


Figure 15-1. Automatic Level Control Block Diagram

15-3. ADJUSTMENTS

To incorporate Option 15 in a 331 counter, please replace paragraph 6-5 with the following adjustment procedure.

PROCEDURE

1. Unplug Source/Amplifier power plug A208J1.
2. Connect a 3 dB pad to the Band III input connector. Apply a +3 dBm, 1.0 GHz, square-wave modulated signal to the pad.
3. Observe the square-wave signal at A204TP1.
4. Adjust A204R61 until the square-wave at TP1 is 90 to 100 mV in amplitude.
5. Reconnect Source/Amplifier power plug.
6. Connect dual trace oscilloscope as follows:

Ch. A	A204TP1 (Mixer Detected Output)
Ch. B	A201FL1 (Power Level Control)
Ext Trig.	A203TP8 (CONVERTER RESET)

7. Set Channel A for DC coupling, 20 mV/cm. Set Channel B for DC coupling, 2 V/cm.
8. Terminate Band III input connector in 50 ohms (a 6 dB or greater pad is adequate).
9. Adjust potentiometers on A202 (Converter Control 2) so the maximum comb line amplitude does not vary appreciably from the levels shown in Table 15-2.
10. Remove the 6 dB terminating pad from the Band III input connector.

Table 15-2. Comb Level Adjustments

ADJUSTMENT	COMB LINE AFFECTED (GHz)	NOMINAL MAXIMUM LEVEL
A202R49	1.0, 1.2	60 mV
A202R86	1.4, 1.6, 1.8	60 mV
A202R50	2.0, 2.2, 2.4, 2.6, 2.8	60 mV
A202R51	3.0, 3.2, 3.4, 3.6, 3.8	60 mV
A202R52	4.0, 4.2, 4.4, 4.6, 4.8	60 mV
A202R53	5.0, 5.2, 5.4, 5.6, 5.8	60 mV
A202R54	6.0, 6.2, 6.4, 6.6, 6.8	60 mV
A202R55	7.0, 7.2, 7.4, 7.6, 7.8	60 mV
A202R56	8.0, 8.2, 8.4, 8.6, 8.8	60 mV
A202R57	9.0, 9.2, 9.4, 9.6, 9.8	60 mV*
* 9.0 GHz only		

NOTE: Additional leveling (if required) obtained by selective addition of R83-96 and R112-121.

15-4. FUNCTIONAL DESCRIPTION

The PIN Driver/Video Amplifier module (A204) consists of two distinct sections: the PIN Diode Attenuator Control Loop, and the Video Amplifier.

Components of the PIN Driver include:

a. PIN Diode Attenuator (A206).
b. Mixer (A205).
c. Current-to-Voltage Converter (A204U1).
d. Loop Amplifier (A204U2).
e. I_{series} Control Circuit (A204Q10-13, Q15, U4).
f. I_{total} Control Circuit (A204CR6, CR7, Q14, U3).

Components of the Video Amplifier include:

a. Four-stage Broadband Amplifier (A204Q1-4).
b. PIN Attenuator Section (A204CR1, CR2, Q5).
c. Four-stage Broadband Amplifier (A204Q6-9).
d. RF Detector (A204CR3, CR4).
e. AGC Loop Amplifier (A204Q16, U5).

The PIN Diode Attenuator Control section is a simple feedback loop. DC current from the Mixer diode is converted to a voltage by U1. This voltage is compared to reference voltage (V_{ref}) at the input of U2. The difference in the two voltages is amplified by U2, and appears at E7. This voltage causes the proper currents to flow from the current generators: I_{series} and I_{total}. These currents determine the magnitude of signal attenuation in the PIN Diode Attenuator (A206).

The I_{series} and I_{total} current generators contain shaping networks that control the ratio of the currents through the series and shunt diodes in the attenuator to provide a fairly constant 50 ohm terminal impedance.

The current shaping network for I_{total} consists of CR6, CR7, R68, and R71. CR6 and CR7 produce an approximately exponential curve, while R68 and R71 produce a linear curve. Their sum determines the shape of the current into the summing node at R75.

In operation, an increase in signal power at the attenuator input results in an increase in the magnitude of DC current from the Mixer diode. The increased current causes the outputs from U1 and U2 to tend positive, increasing I_{total} while decreasing I_{series}. This produces an increase in the current through the shunt diode, and a decrease in the current through the series diodes, in a ratio which maintains a 50 ohm terminal impedance. This action decreases the magnitude of change in signal power which appears at the Mixer diode.

The Video Amplifier section amplifies the difference frequency produced by the Mixer, and applies it to Converter Control 1 (A203).

The circuit consists of eight essentially identical gain blocks and an automatic gain control. Overall gain of the Video Amplifier is nominally 56 dB, with a frequency range of 25 MHz to 275 MHz.

A typical gain block includes a single broadband transistor amplifier stabilized by series and shunt feedback, and an output matching inductor.

The AGC portion of the amplifier consists of RF level detector CR3 and CR4, loop amplifier U5, PIN Diode current driver Q16, emitter follower Q5, and PIN Attenuator diodes CR1 and CR2. The reference voltage in the AGC loop sets the maximum output power level for the Video Amplifier at 0 to +1 dBm.

15-5. PARTS LIST

Mixer (A205) and Attenuator (A206) are factory matched to PIN Driver/Video Amplifier (A204), and must be replaced as a *matched set* (EIP P/N 2010061). Consult factory or regional sales representative for service or replacement details for any of these assemblies.

A204/Option 15 – Video Amplifier With Automatic Input Level Control

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
A204/15	Video Ampl/Auto Level Control	2020045			
C1	Mica, 470pF	2250018	1	DM15CD471JO	72136
C2	Cer, .01μF	2150003	48	TG-S10	56289
C3	Cer, S.A.T. (2.2pF max.)	2160999	1	301000C0X0XXXX	72982
C4	C2				
C5	Mica, 180pF	2250006	8	DM15CD181JO	72136
C6 thru C9	C2				
C10	C5				
C11 thru C14	C2				
C15	C5				
C16 thru C19	C2				
C20	Mica, 27pF	2250012	1	DM15CD270JO	72136
C21	Mica, 200pF	2250009	1	DM15CD201JO	72136
C22	C2				
C23	Cer, .001μF	2150001	2	5GA-D10	56289
C24	C2				
C25	C2				
C26	Not Used				
C27	C23				
C28 thru C30	C2				
C31	C5				
C32 thru C35	C2				
C36	C5				
C37 thru C40	C2				
C41	C5				
C42 thru C45	C2				
C46	C5				
C47	C2				

A204/Option 15 – Video Amplifier With Automatic Input Level Control (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
C48	C2				
C49	Tant, 10μF, 25V	2300029	2	TAG-20-10/25(M)	14433
C50	Cer, 1pF	2160002	1	301000C0K0109C	72982
C51	Cer, 8.2pF	2160015	1	301000C0H0829C	72982
C52 thru C55	C2				
C56	C5				
C57 thru C64	C2				
C65	Mica, 120pF	2250027	1	DM1_CD121JO	72136
C66	Mica, 100pF	2250002	2	DM15CD101JO	72136
C67	C2				
C68	C49				
C69	C2				
C70	C66				
CR1	Pin	2710022	2	MA47110	96341
CR2	CR1				
CR3	Hot Carrier	2710004	3	FH1100	EIP
CR4	CR3				
CR5	Not Used				
CR6	CR3				
CR7	ZNR, 2.4V	2704370	1	1N4370	04713
CR8	Rectifier	2704001	1	1N4001	04713
CR9	G.P.	2704154	1	1N4154	07263
L1	Ind., 2.2μH	3510005	1	DD-2.20	72259
L2	Wire buss, 22 AWG	5460008	A/R	22-122-T/C-S	
L3 thru L9	Part of Board				
L10	Ind., .33μH	3510007	1	1025-08	99800
L11 thru L20	Part of Board				
Q1	NPN, RF	4710026	2	NE73432B	
Q2	NPN, 2N5179 – Red	4710011	5	M/F4705179	EIP
Q3	Q2				
Q4	NPN SEL, 2N5179 – Yellow	4710012	4	M/F4705179	EIP
Q5	Q4				

A204/Option 15 – Video Amplifier With Automatic Input Level Control (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
Q6	Q2				
Q7	Q2				
Q8	Q4				
Q9	Q1				
Q10	NPN, GP	4704124	3	2N4124	04713
Q11	Q10				
Q12	PNP, GP	4704126	3	2N4126	04713
Q13	Q12				
Q14	Q10				
Q15	Q12				
Q16	Q2				
Q12	Q4				
R1	Met Ox, 1.3K, 2%	4130132	2	C4/2%/1.3K	24546
R2	Met Ox, 200 ohms, 2%	4130201	1	C4/2%/200	24546
R3	Met Ox, 470 ohms, 2%	4130471	3	C4/2%/470	24546
R4	Met Ox, 2.4K, 2%	4130242	7	C4/2%/2.4K	24546
R5	Met Ox, 56 ohms, 2%	4130560	6	C4/2%/56	24546
R6	CBN FLM, 8.2 ohms, 5%	4120008	4	R25-8.2-5%-¼W	
R7	Met Ox, 910 ohms, 2%	4130911	6	C4/2%/910	24546
R8	Comp, 2.2K, 5%	4010222	3	RC07GF222J	81349
R9	Met Ox, SAT (20 ohms nom.)	4130999	7	C4/2%/20Ω Nom.	24546
R10	Met Ox, 620 ohms, 2%	4130621	7	C4/2%/620	24546
R11	R4				
R12	R5				
R13	R6				
R14	R7				
R15	R9				
R16	R10				
R17	R4				
R18	R5				
R19	Met Ox, 10 ohms, 2%	4130100	3	C4/2%/10	24546
R20	R7				
R21	Comp, 510 ohms, 5%	4010511	1	RC07GF511	81349
R22	R9				
R23	R10				
R24	Met Ox, 51 ohms, 2%	4130510	4	C4/2%/51	24546
R25	R10				
R26	Comp, 1.1K, 5%	4010112	1	RC07GF112J	81349
R27	Met Ox, 120 ohms, 2%	4130121	2	C4/2%/120	24546
R28	Comp, 220 ohms, 5%	4010221	1	RC07GF221J	81349
R29	CBN FLM, 5.6 ohms, 5%	4120004	2	R25-5.6-5%-¼W	
R30	R27				

A204/Option 15 – Video Amplifier With Automatic Input Level Control (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R31	R4				
R32	R29				
R33	R7				
R34	R6				
R35	R9				
R36	R10				
R37	R4				
R38	R5				
R39	R6				
R40	R7				
R41	Comp, 1K, 5%	4010102	4	RC07GF102J	81349
R42	R9				
R43	R10				
R44	R4				
R45	R5				
R46	R7				
R47	R19				
R48	R9				
R49	R10				
R50	R4				
R51	R5				
R52	Met Ox, 820 ohms, 2%	4130821	2	C4/2%/821	24546
R53	R24				
R54	R19				
R55	R24				
R56	R3				
R57	Comp, 120 ohms, 5%	4010121	1	RC07GF121J	81349
R58	R24				
R59	Met Ox, 1.5K, 2%	4130152	1	C4/2%/1.5K	24546
R60	Met Ox, 2.7K, 2%	4130272	1	C4/2%/2.7K	24546
R61	Var, 100K	4250008	2	72XWR100K	73138
R62	Met Ox, 13K, 2%	4130133	1	C4/2%/13K	24546
R63	Met Ox, 10K, 2%	4130103	4	C4/2%/10K	24546
R64	Met Ox, 390 ohms, 5%	4010391	1	RC07GF390J	81349
R65	R41				81349
R66	R41				81349
R67	Comp, 47K, 5%	4010473	2	RC07GF473J	81349
R68	R61				
R69	Comp, 8.2K, 5%	4010822	2	RC07GF822J	81349
R70	R69				
R71	Comp, 5.6 ohms, 5%	4010569	1	RC07GF569J	81349
R72	Comp, 16K, 5%	4010163	2	RC07GF163J	81349
R73	R72				

A204/Option 15 – Video Amplifier With Automatic Input Level Control (Continued)

REF DES	DESCRIPTION	EIP NO.	UNITS PER ASSY	TYP MFG NO.	TYP FSCM NO.
R74	R41				
R75	Met Ox, 1.2K, 2%	4130122	1	C4/2%/1.2K	24546
R76	R63				
R77	Met Ox, 91 ohms, 2%	4130910	1	C4/2%/91	24546
R78	Met Ox, 16K, 2%	4130163	1	C4/2%/16K	24546
R79	R1				
R80	Met Ox, 2.2K, 2%	4130222	2	C4/2%/2.2K	24546
R81	R63				
R82	R63				
R83	Met Ox, 1K, 2%	4130102	1	C4/2%/1K	24546
R84	R52				
R85	Var, 1K	4250003	1	72XWR1K	73138
R86	Met Ox, 680 ohms, 2%	4130681	1	C4/2%/680	24546
R87	Comp, 10K	4010103	1	RC07GF103J	81349
R88	Met FLM, 8.66K, 1%	4068661	2	RN55D8661F	81349
R89	R88				
R90	Comp, 470 ohms, 5%	4010471	1	RC07GF471J	81349
R91	Met Ox, 3.9K, 2%	4130392	2	C4/2%/3.9K	24546
R92 thru R95	Comp, 24 ohms, 5%	4010240	4	RC07GF240J	81349
R96	R3				
R97	Met Ox, 12K, 2%	4130123	1	C4/2%/12K	24546
R98	Met Ox, 100 ohms, 2%	4130101	1	C4/2%/100	24546
R99	Comp, 68 ohms, 5%	4010680	1	RC07GF680J	81349
R100	R91				
R101	R67				
R102	Met Ox, 5.6K, 2%	4130562	1	C4/2%/5.6K	24546
R103	Met Ox, 7.5K, 2%	4130752	1	C4/2%/7.5K	24546
R104	R8				
R105	R8				
R106	R9				
R107	Met Ox, 6.2K, 2%	4130622	1	C4/2%/6.2K	24546
R108	Met Ox, 30K, 2%	4130303	1	C4/2%/30K	24546
R109	Comp, 470K, 5%	4010474	1	RC07GF474J	81349
R110	Met Ox, 390 ohms, 2%	4130391	1	C4/2%/390	24546
R111	R80				
U1	Op Amp, Hi Slew Rate	3040001	1	OP-01CJ	
U2 thru U4	Op Amp	3040741	3	LM741CN	0000X
U5	Op Amp, Hi Slew Rate	3041741	1	MC1741SCP1	0000X
A205	Part of Assy 2010061				
A206	Part of Assy 2010061				

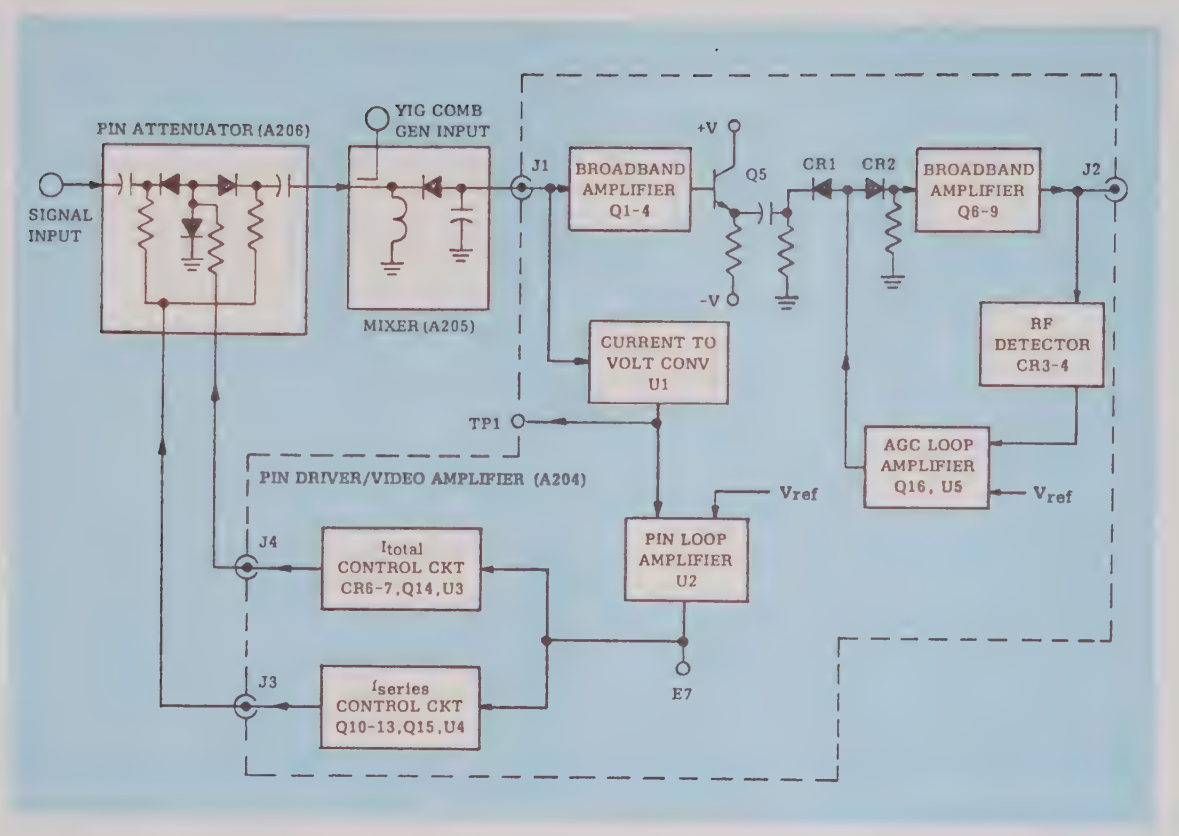
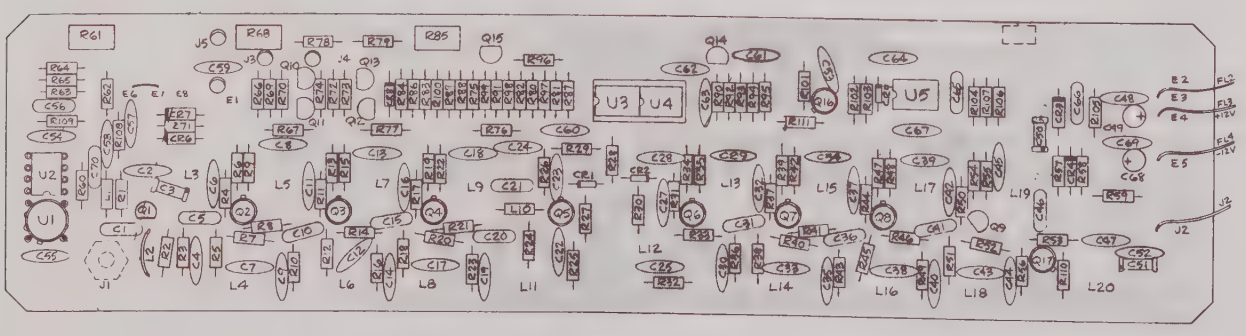
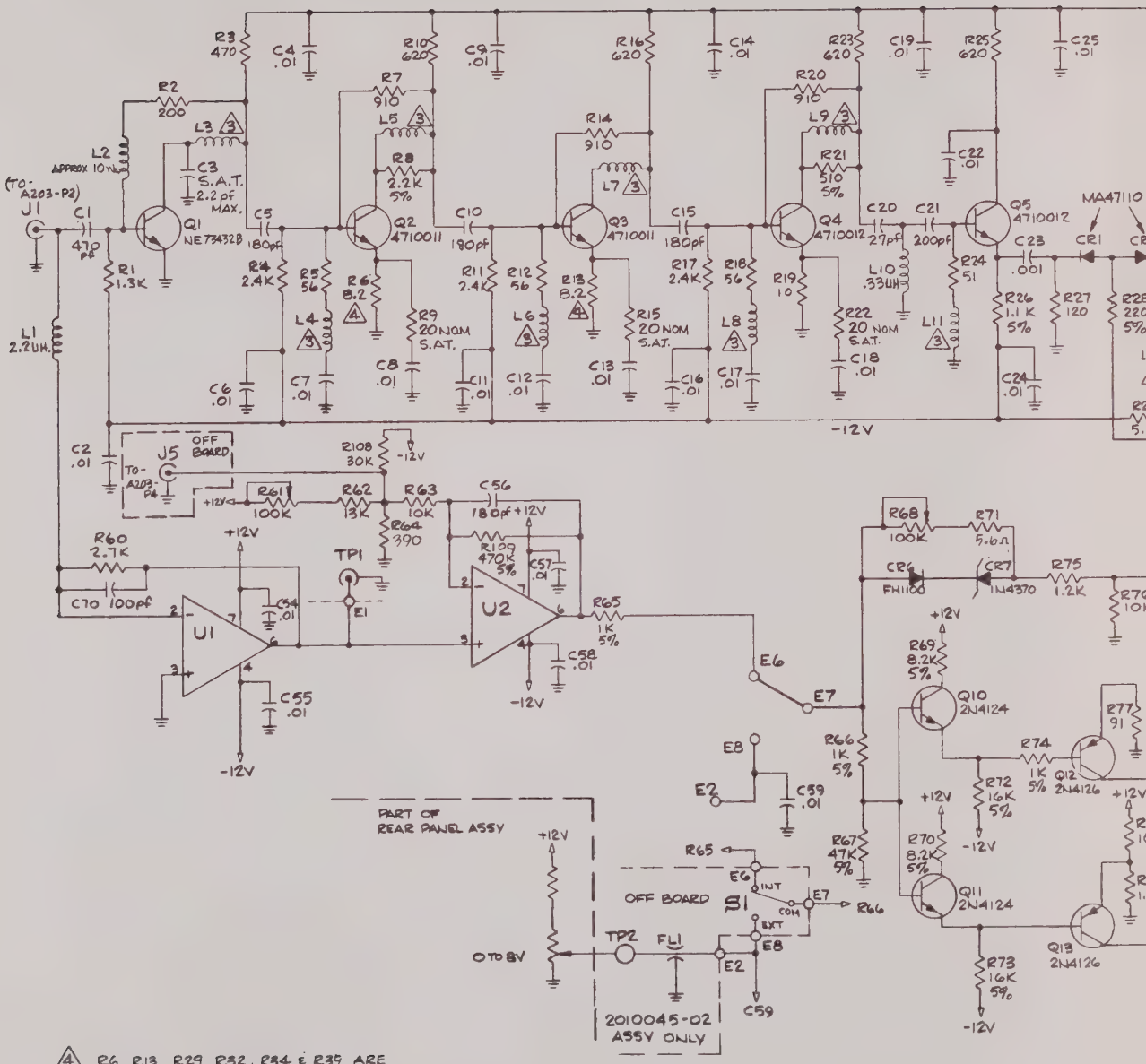


Figure 15-2. Option 15 Video Amplifier Functional Diagram



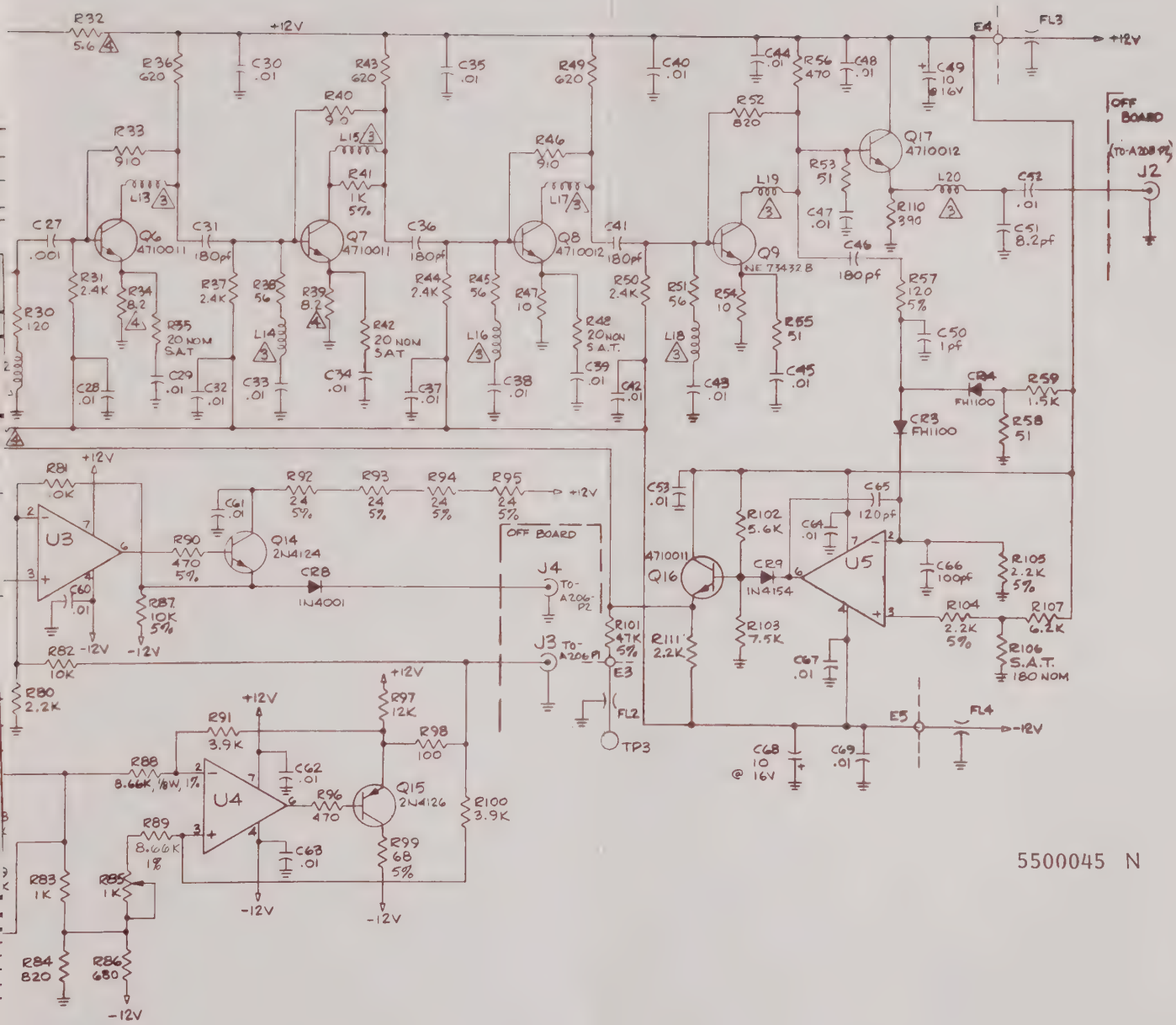
2020045 W

Figure 15-3. Component Locator



4 R6, R13, R29, R32, R34 & R39 ARE CARBON FILM RESISTORS, 1/4W, ±5%.

3 PART OF P.C. BOARD.



5500045 N

Figure 15-4. Schematic Diagram

OPTION 31
PROGRAMMING

31-1. DESCRIPTION

Option 31 gives the user the ability to remotely program the front panel commands HOLD, RESET, and TEST. This option also allows remote programming of counter reset (initiates a new reading without resetting the converter), and converter sweep presets. Remote HOLD, RESET, and TEST are enabled by the LOCAL/REMOTE line while counter reset and converter presets are always enabled. All inputs are TTL compatible. All inputs, except counter reset, are activated by a TTL low or ground.

31-2. CONVERTER PRESETS

Increments of 200 MHz may be programmed by pulling the appropriate inputs low using standard 1-2-4-8 BCD code. These inputs drive Converter Control 2 inverters, A202U7 and U9, to preset the DCU's of DAC1 on A202.

31-3. OPERATION

For proper Converter operation, the sweep function must operate. This requires that the frequency to be measured be at a minimum of 275 MHz above the preset frequency. The preset number must be at least 275 MHz above any other frequencies present. Under these conditions the Converter Presets may be used to speed acquisition time, and to measure a signal in the presence of a lower frequency signal.

TO OPERATE:

- Enter preset frequency in counter with programming requirement considerations.
- Press RESET button.

EXAMPLE

To measure 8 GHz signal in presence of 4 GHz signal (both signals above minimum sensitivity of counter), program counter for 7 GHz and press RESET button. Counter will begin sweep at 7 GHz and lock on 8 GHz signal.

31-4. REMOTE HOLD, RESET, TEST, and RESET COUNTER

Reset Counter goes directly to the counter reset generator. A high-going transition causes the counter to take a new reading without affecting the converters. HOLD, RESET, and TEST each go through a 2:1 multiplexer used as a switch. In the local mode the front panel switches are enabled, controlling the counter functions. In the remote mode the multiplexers enable the remote functions. A low-level on the TEST and HOLD inputs activate these functions, while a low-going transition on the RESET input generates a reset. If the counter is not in HOLD the front panel sample rate pot controls the sample rate.

The connector used is an Amphenol type 57-40500, 50 pin female. The mating connector is an Amphenol 57-30500, 50 pin male.

Table 31-1. J3 Contact Grounding for Programming

A1J3 Pin No.	FUNCTION
4	$\overline{\text{Hold}}$
5	$\overline{\text{Reset}}$
6	$\overline{\text{Test}}$
7	Counter Reset
16	10^8 B (200 MHz)
17	10^8 C (400 MHz)
18	10^8 D (800 MHz)
19	10^9 A (1 GHz)
20	10^9 B (2 GHz)
21	10^9 C (4 GHz)
22	10^9 D (8 GHz)
23	10^{10} A (10 GHz
24	Ground
25	+5 Vdc

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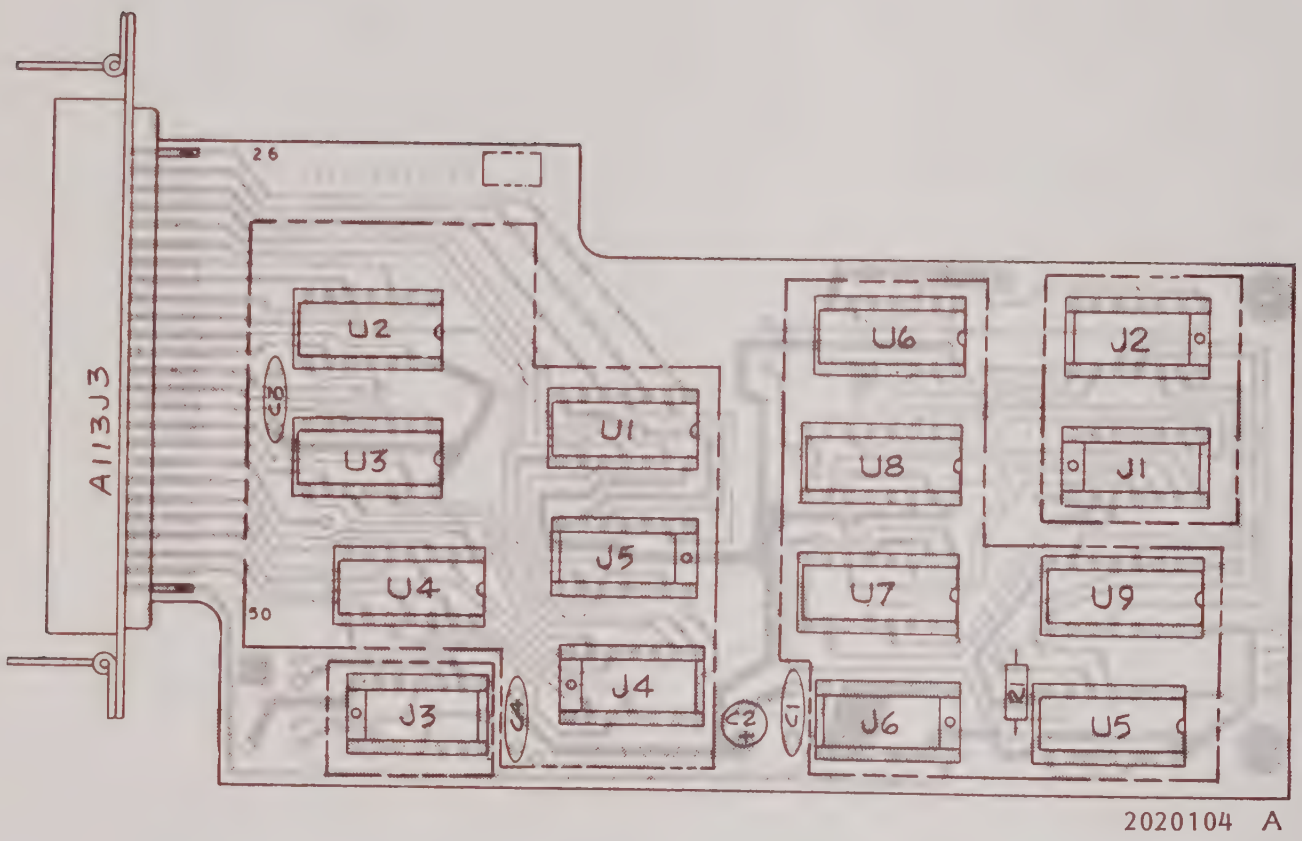
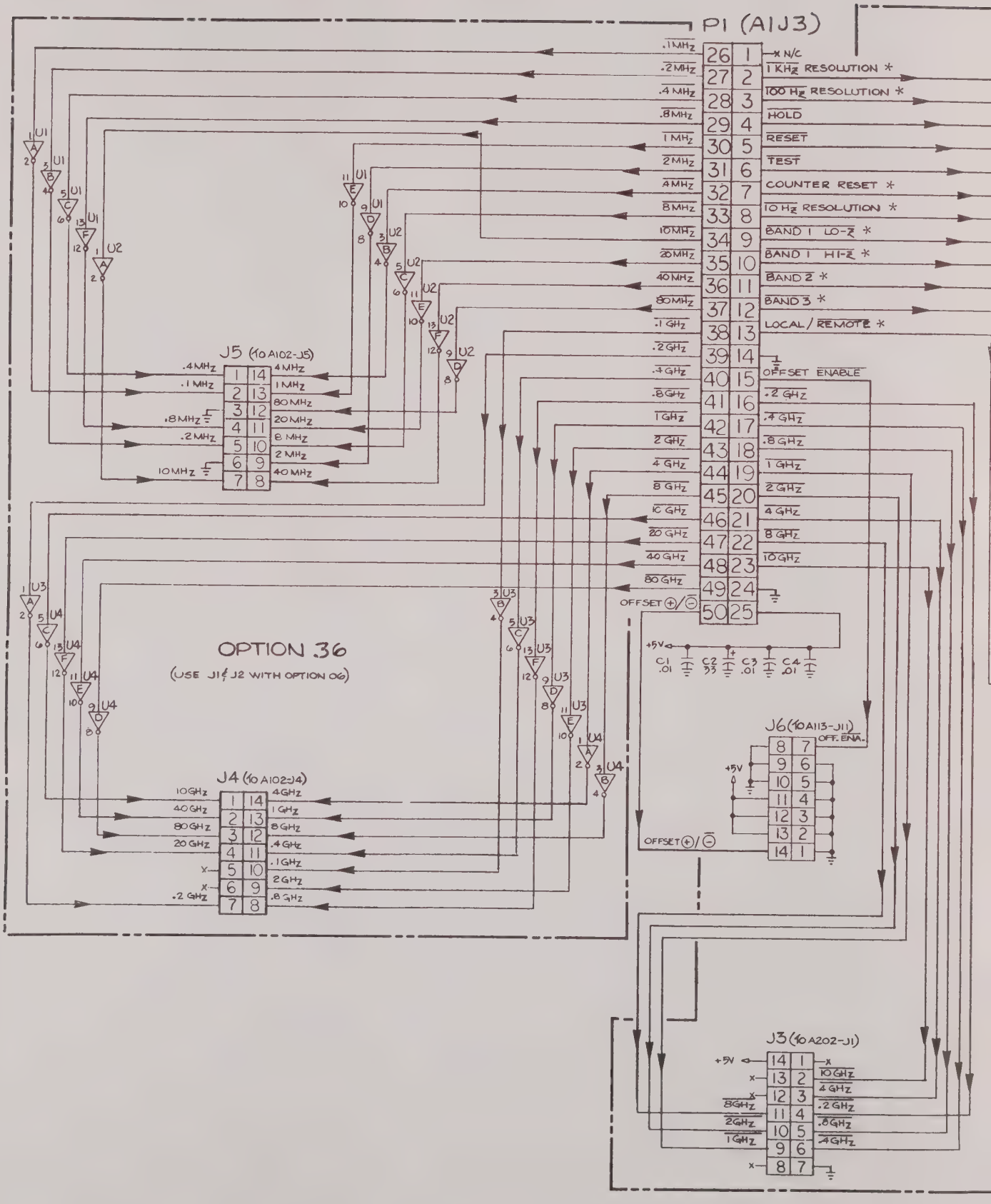
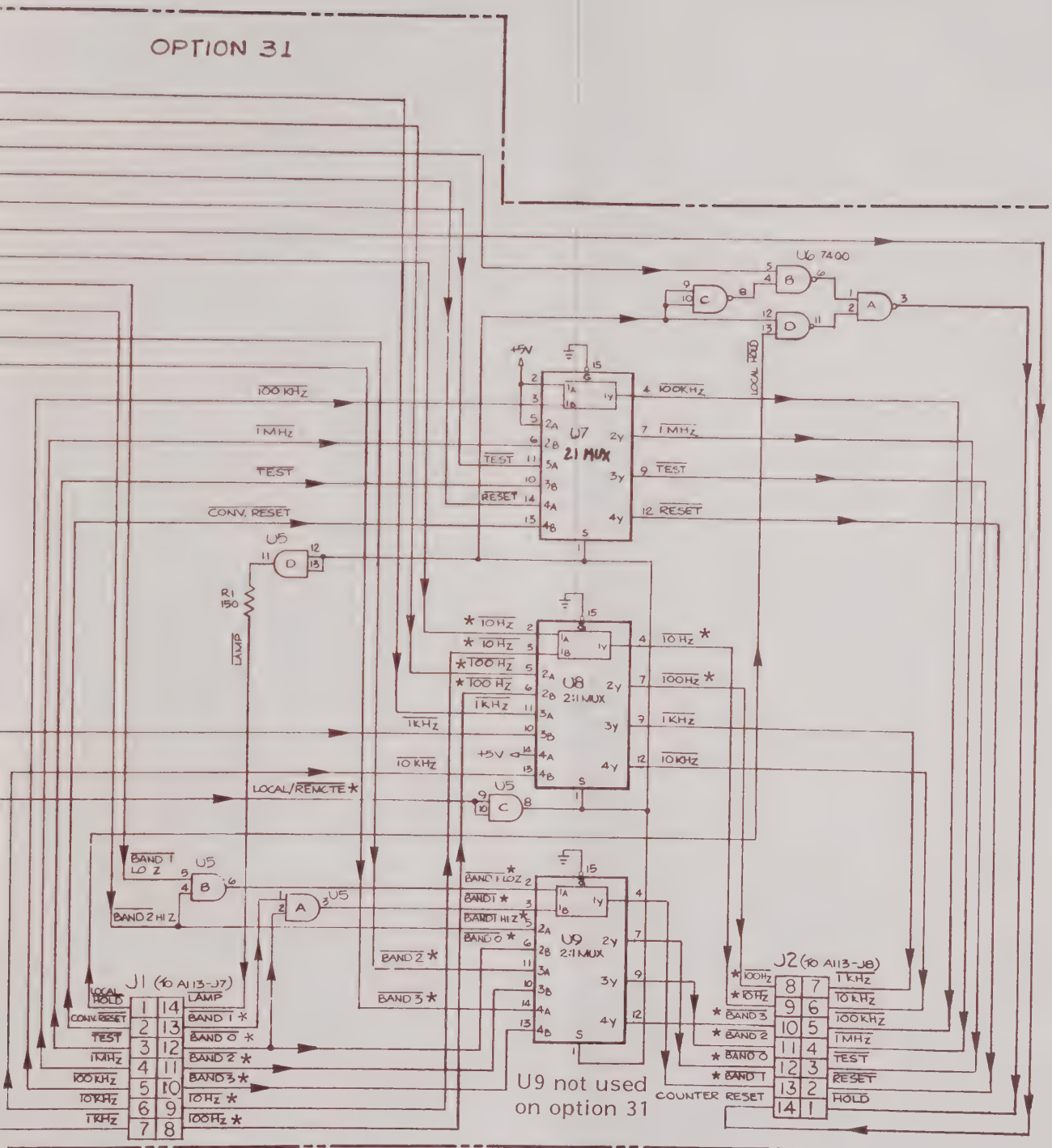


NOTE: COMPOSITE PCB ASSEMBLY FOR PROGRAMMING OPTION BOARD. ONLY A PORTION OF COMPONENTS SHOWN MAY BE USED ON ANY ONE OPTION.

Figure 31-1. Component Locator, A115


P1 (A1J3)
.1 MHz
.2 MHz
.4 MHz
.8 MHz
1 MHz
2 MHz
4 MHz
8 MHz
10 MHz
20 MHz
40 MHz
80 MHz
.1 GHz
.2 GHz
.4 GHz
.8 GHz
1 GHz
2 GHz
4 GHz
8 GHz
10 GHz
20 GHz
40 GHz
80 GHz
N/C
1 KHz RESOLUTION *
100 Hz RESOLUTION *
HOLD
RESET
TEST
COUNTER RESET *
10 Hz RESOLUTION *
BAND 1 LO-Z *
BAND 1 HI-Z *
BAND 2 *
BAND 3 *
LOCAL / REMOTE *
OFFSET ENABLE
OFFSET ⊕/⊖
+5V
C1 .01
C2 33
C3 .01
C4 .01
J5 (TO A102-J5)
J4 (TO A102-J4)
J6 (TO A113-J1)
OFF. ENA.
OPTION 36
(USE J1 & J2 WITH OPTION 06)
J3 (TO A202-J1)



5500104 A

NOTE: COMPOSITE SCHEMATIC FOR PROGRAMMING OPTION PC BOARD. ONLY A PORTION OF COMPONENTS SHOWN MAY BE USED FOR ANY ONE OPTION.

* Not used with model 331

Figure 31-2. Schematic Diagram

OPTION 32
YIG PRESET THUMBWHEEL

32-1. DESCRIPTION

This option allows the user to program the sweep starting frequency for decreased acquisition time, or to provide signal selectivity with a multiple frequency input. Preset frequency increments of 200 MHz can be set by the thumbwheel switch.

32-2. OPERATION

For proper Converter operation, the sweep function must operate. This requires that the frequency to be measured be at a minimum of 275 MHz above the preset frequency. The preset number must be at least 275 MHz above any other frequencies present. Under these conditions the Converter Presets may be used to speed acquisition time, and to measure a signal in the presence of a lower frequency signal.

TO OPERATE

- Enter preset frequency in counter with programming requirement considerations.
- Press RESET button.

EXAMPLE

To measure 8 GHz signal in presence of 4 GHz signal (both signals above minimum sensitivity of counter), program counter for 7 GHz and press RESET button. Counter will begin sweep at 7 GHz and lock on 8 GHz signal.

32-3. REMOTE HOLD, RESET, TEST, and RESET COUNTER

Reset Counter goes directly to the counter reset generator. A high-going transition causes the counter to take a new reading without affecting the converters. HOLD, RESET, and TEST each go through a 2:1 multiplexer used as a switch. In the local mode the front panel switches are enabled, controlling the counter functions. In the remote mode the multiplexers enable the remote functions. A low-level on the TEST and HOLD inputs activate these functions, while a low-going transition on the RESET input generates a reset. If the counter is not in HOLD the front panel sample rate pot controls the sample rate.

The connector used is an Amphenol type 57-40500, 50 pin female. The mating connector is an Amphenol 57-30500, 50 pin male.

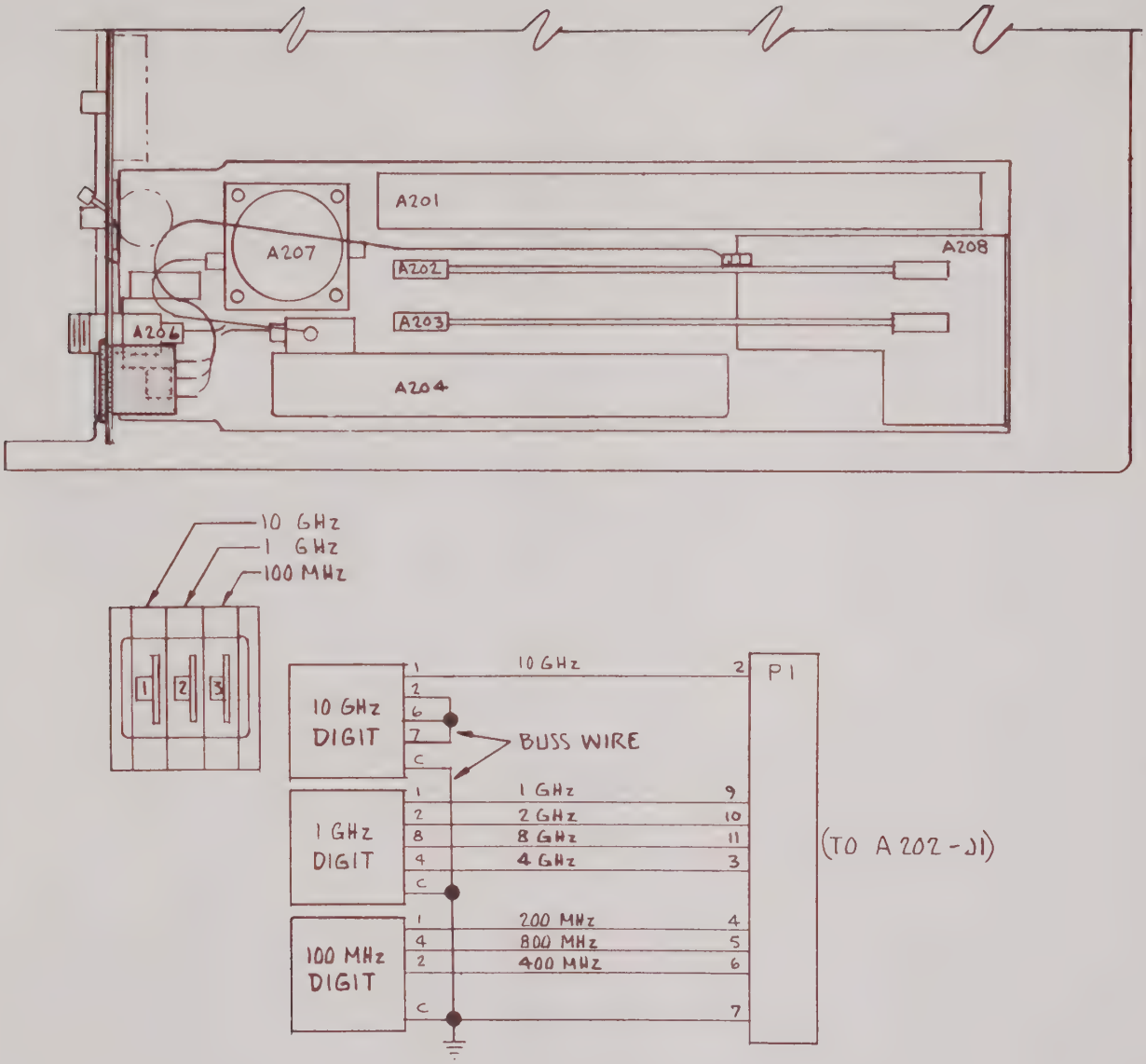


Figure 32-1. Component Locator and Wiring Diagram

36-1. GENERAL DESCRIPTION

This option allows the displayed reading of any frequency to be increased or decreased by any number in 100 kHz increments.

For positive offsets, the desired number may be programmed directly on 24 input lines (4-line BCD code on each of six digits). Activating the $\overline{\text{OFFSET ENABLE}}$ command will then cause the reading to be offset by the programmed frequency.

Negative offsets require that the nines complement of the number be programmed and that the $\overline{\text{OFFSET MINUS}}$ command be activated. The nines complement of a number is obtained by subtracting the number from 99.9999 GHz.

All inputs are programmed by ground contact closure or application of a TTL "0" level. Pin connections are shown in Table 36-1.

36-2. CIRCUIT DESCRIPTION

Circuitry required for the option is contained on two PC boards. Programming Option Board A115 contains the inverters used as buffers for the input information. Offset Control Unit A100 contains the remaining control circuitry.

The six digit offset input is used to directly preset the six DCUs on Count Chain 2 (A102). This then requires that the 3 MSD information from the Converter must be serially added to the preset information. This is the major function of the Offset Control unit.

The second function of the unit is to provide a single pulse to the 100 kHz DCU of A102 during negative offset.

During $\overline{\text{SEQUENCE GENERATOR "0,"}}$ 3 MSD information from the Converter is preset into U6, U7, and U8. The $\overline{\text{OFFSET LOAD}}$ command is generated (U2 pin 6) and, if $\overline{\text{OFFSET MINUS}}$ is low (negative offset), U4B is set.

At $\overline{\text{SEQUENCE GENERATOR "1,"}}$ U3A is enabled and divides the input 2.5 MHz clock to 1.25 MHz. U3B inhibits the sequence generator and enables U4A. The first clock pulse triggers U4A which activates the GATE X 100 MHz signal and operates a single ADD X 100 kHz pulse if negative offset is selected. Clock pulses then simultaneously appear at the ADD X 100 MHz output and the $\overline{\text{COUNT DOWN}}$ input to U6. Pulses continue until U6, U7, and U8 have counted down to zero. U3B is then reset, which in turn resets U4A, ends the cycle, and removes the $\overline{\text{SEQUENCE GENERATOR INHIBIT}}$.

Programming connector type: Amphenol 57-40500, 50 pin female. Mating connector: Amphenol 57-30500, 50 pin male.

Table 36-1. A1J3 Contact Grounding

J3 Pin	Function	J3 Pin	Function
14	Ground	38	10^8 A (100 MHz)
15	Offset $\overline{\text{Enable}}$	39	10^8 B (200 MHz)
26	10^5 A (100 kHz)	40	10^8 C (400 MHz)
27	10^5 B (200 kHz)	41	10^8 D (800 MHz)
28	10^5 C (400 kHz)	42	10^9 A (1 GHz)
29	10^5 D (800 kHz)	43	10^9 B (2 GHz)
30	10^6 A (1 MHz)	44	10^9 C (4 GHz)
31	10^6 B (2 MHz)	45	10^9 D (8 GHz)
32	10^6 C (4 MHz)	46	10^{10} A (10 GHz)
33	10^6 D (8 MHz)	47	10^{10} B (20 GHz)
34	10^7 A (10 MHz)	48	10^{10} C (40 GHz)
35	10^7 B (20 MHz)	49	10^{10} D (80 GHz)
36	10^7 C (40 MHz)	50	Offset Plus/$\overline{\text{Minus}}$
37	10^7 D (80 MHz)		

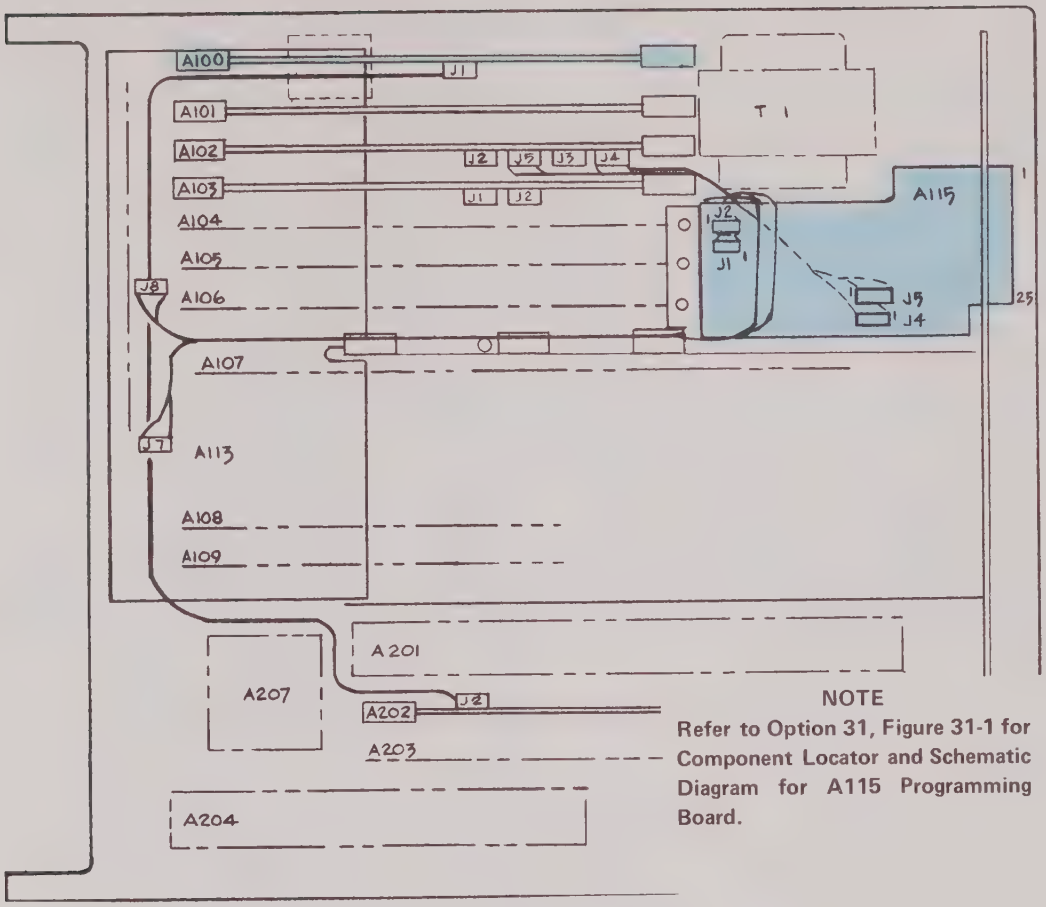


Figure 36-1. Assembly Locator and Cable Diagram

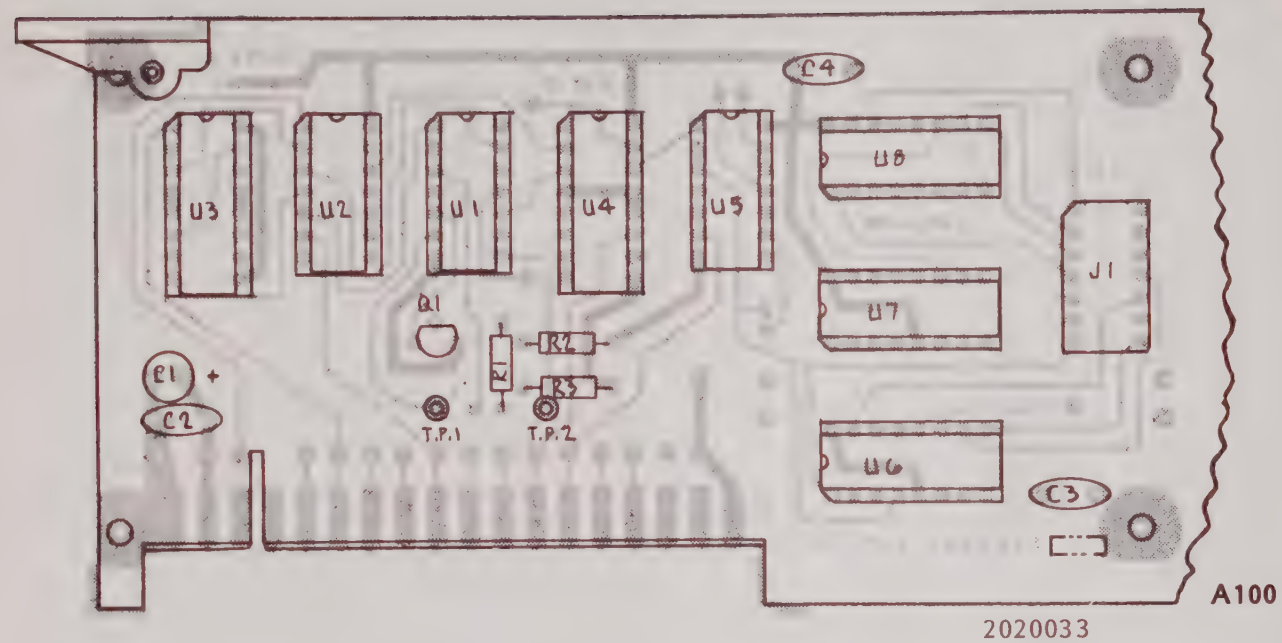
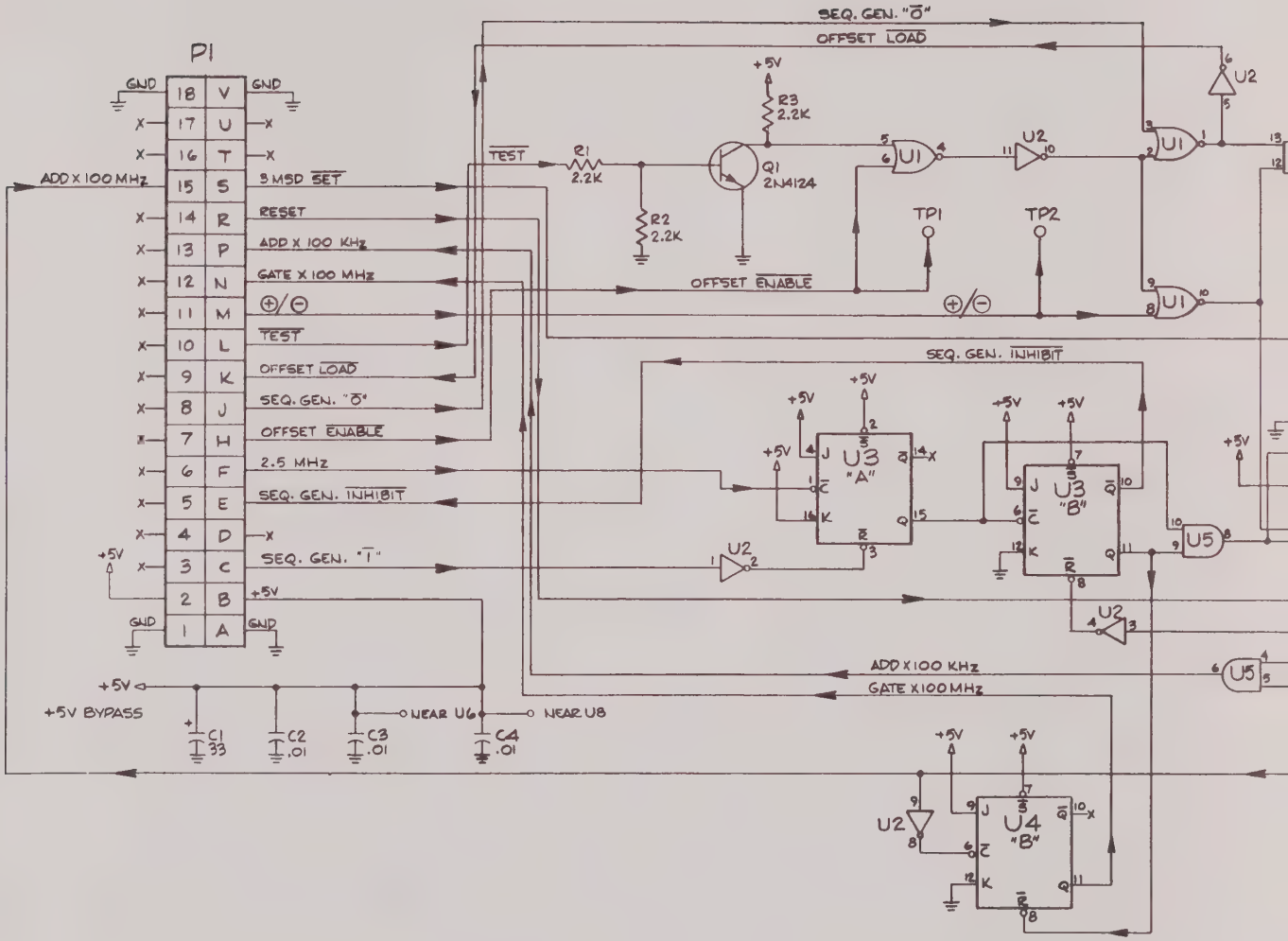


Figure 36-2. Component Locator

5580007


P1
GND
18 V
17 U
16 T
15 S
14 R
13 P
12 N
11 M
10 L
9 K
8 J
7 H
6 F
5 E
4 D
3 C
2 B
1 A
ADD X 100 MHz
3 MSD SET
RESET
ADD X 100 KHz
GATE X 100 MHz
TEST
OFFSET LOAD
SEQ. GEN. "Ō"
OFFSET ENABLE
2.5 MHz
SEQ. GEN. INHIBIT
SEQ. GEN. "T"
+5V
+5V BYPASS
C1 33
C2 .01
C3 .01
C4 .01
NEAR U6
NEAR U8
R1 2.2K
R2 2.2K
R3 2.2K
Q1 2N4124
TP1
TP2
U1
U2
U3 "A"
U3 "B"
U4 "B"
U5

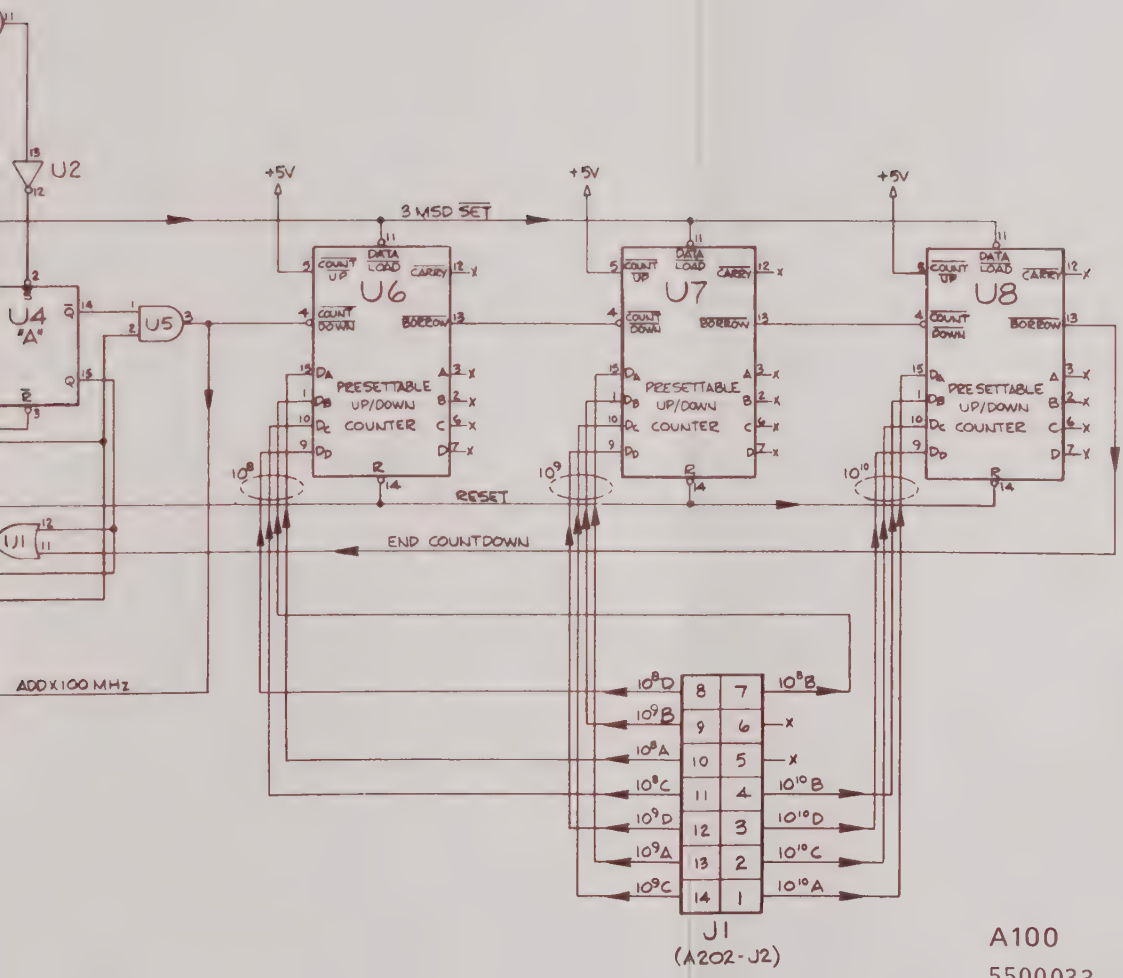


Figure 36-3. Schematic Diagram

39-1. DESCRIPTION

This assembly provides binary coded decimal outputs to the rear panel of the counter corresponding to the applied input frequency. A $\overline{\text{PRINT}}$ command indicates the presence of valid data, while an INHIBIT input is available to allow the user to prevent the information from being altered. Refer to Table 39-2 for rear panel connections.

Each output line from the latches associated with the counting chain (A102, A103) then feeds through an inverter to the rear panel Digital Output Connector J2.

A positive INHIBIT level (+2 to +50V) turns on Q1. This in turn, generates a $\overline{\text{SEQUENCE INHIBIT}}$ command to prevent the counter from continuing its sequence. This command allows the user to prevent stored information from being altered.

Table 39-1. Specifications

BCD Code	1 - 2 - 4 - 8
Format	8 data digits in parallel form
"0" State Level	0 to 0.4V, 5 mA current sink capability
"1" State Level	+5V, 2k ohm source impedance
Negative Ref	Ground
Positive Ref	+5V, 22 ohm source impedance
Print Command	+5V to 0V step, fall time 1 microsecond, 20 microsecond width. 2k ohm source impedance.
Hold Off Requirement	Maximum: 50V; minimum: 2V.

Table 39-2. A1J2 Contact Grounding

Pin No.	Function	Pin No.	Function	Pin No.	Function
5	10^3 A	19	10^{10} A	39	10^7 D
6	10^3 B	20	10^{10} B	40	10^8 C
7	10^4 A	22	Inhibit	41	10^8 D
8	10^4 B	24	– Ref	42	10^9 C
9	10^5 A	25	+ Ref	43	10^9 D
10	10^5 B	30	10^3 C	44	10^{10} C
11	10^6 A	31	10^3 D	45	10^{10} D
12	10^6 B	32	10^4 C	48	Print Comm.
13	10^7 A	33	10^4 D		
14	10^7 B	34	10^5 C	49	No Connec.
15	10^8 A	35	10^5 D		
16	10^8 B	36	10^6 C	50	Ground
17	10^9 A	37	10^6 D		
18	10^9 B	38	10^7 C		

NOTE: The 10^3 bit is the least significant digit, and corresponds to the 1 kHz output. A, B, C, and D, are the 1, 2, 4, and 8, bits of each binary coded decimal output digit.

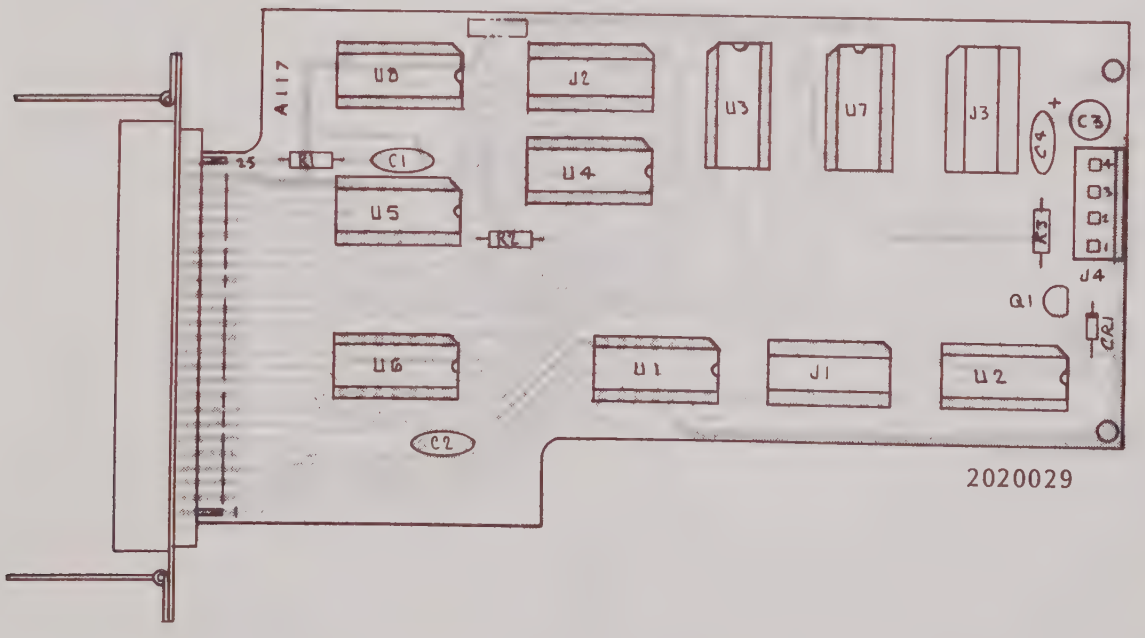
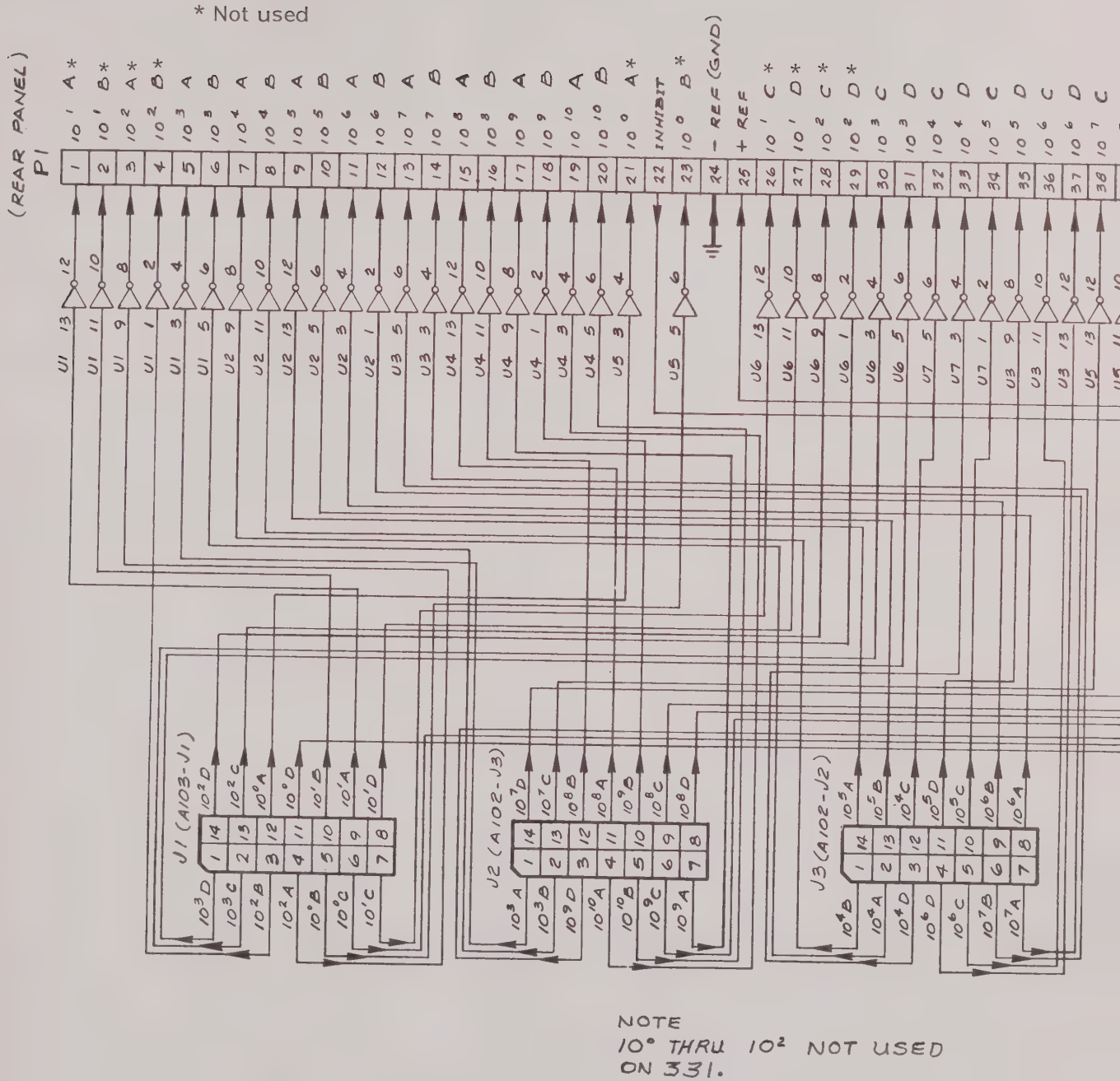
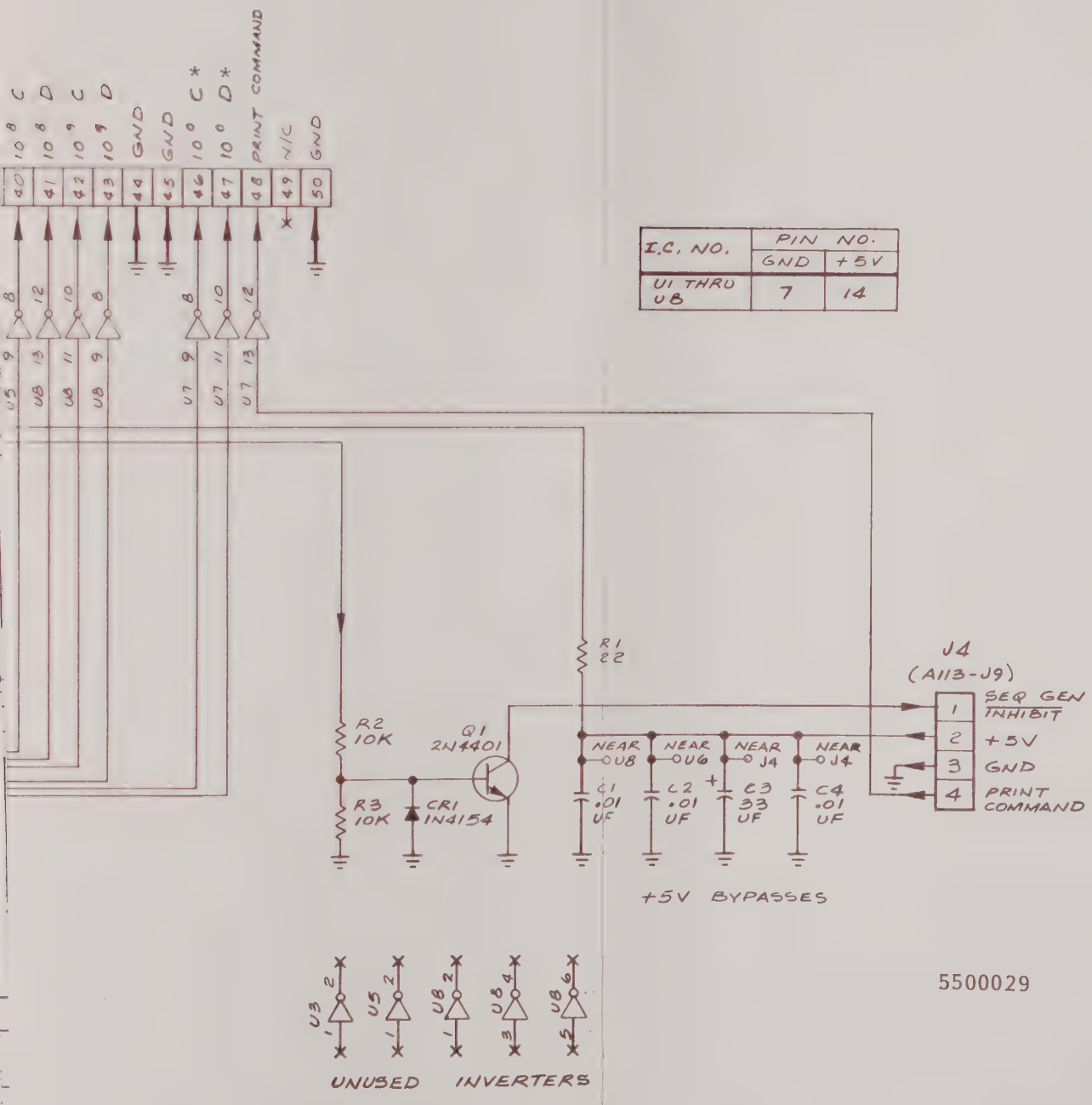


Figure 39-1. Component Locator

5580007



NOTE
10^0 THRU 10^2 NOT USED
ON 331.



5500029

Figure 39-2. Schematic Diagram

OPTION 40
REAR PANEL INPUTS

40-1. DESCRIPTION

The Converter assembly is reversed, end-for-end, to place the input connector at rear panel. All specifications remain the same as those stated for front panel connectors.

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